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# **SCA32GE13H1F1C-56B**

**288-Pin DDR5 Unbuffered DIMM(X72,ECC)  
EU RoHS Compliant**

## **Data Sheet**

**Rev. A**

| Revision History |          |                                              |
|------------------|----------|----------------------------------------------|
| Date             | Revision | Subjects (major changes since last revision) |
| 2025-01          | A        | Initial Release                              |

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# 1 Overview

This chapter gives an overview of the 288-pin DDR5 ECC UDIMM product family and describes its main characteristics.

## 1.1 Features

- 288-Pin PC5-5600 DDR5 ECC UDIMM
- On-DIMM SPD EEPROM with hub function and integrated temperature sensor (TS)
- On-DIMM Power management integrated circuit (PMIC)
- Frequency/CAS latency: 0.357ns @ CL = 46 (DDR5-5600)
- VDD = VDDQ = 1.1V
- VPP = 1.8V
- On-die, internal, adjustable VREF generation for DQ, CA, CS
- 32 internal banks: 8 groups of 4 banks each
- 16n-bit prefetch architecture
- Gold edge contacts
- Halogen-free
- Fly-by topology
- Terminated clock, control, command and address bus
- Anti-Sulfurated Option

**Table 1 - Module Performance Table**

| UnilC Speed Code        |           | -56B      | Unit     | Note |
|-------------------------|-----------|-----------|----------|------|
| DRAM Speed Grade        | DDR5      | -5600     |          |      |
| CAS-RCD-RP latencies    |           | -46-45-45 | $t_{CK}$ |      |
| Min. RAS-CAS-Delay      | $t_{RCD}$ | 16        | ns       |      |
| Min. Row Precharge Time | $t_{RP}$  | 16        | ns       |      |
| Min. Row Active Time    | $t_{RAS}$ | 32        | ns       |      |
| Min. Row Cycle Time     | $t_{RC}$  | 48        | ns       |      |

## 1.2 Description

The UnilC 32GB module family are ECC UDIMM with 31.25mm height based on DDR5 technology.

DIMMs intended for mounting into 288-pin connector sockets.



**Table 2 - Ordering Information**

| Product Type               | Compliance Code <sup>1)</sup> | Description | SDRAM Technology |
|----------------------------|-------------------------------|-------------|------------------|
| <b>PC5-5600 (46-45-45)</b> |                               |             |                  |
| SCA32GE13H1F1C-56B         | 32GB 2R×8 PC5-5600-46-45-45   | 2Ranks      | 16Gbit (×8)      |

- 1) This describes the speed grade, for example " PC5-5600-46-45-45" where 5600 means DIMM modules with 5600MT/s data rate and "46-45-45" means Column Address Strobe (CAS) latency=46, Row Column Delay (RCD) latency = 45 and Row Precharge (RP) latency = 45.

**Table 3 - Address Format**

|                                      |                       |
|--------------------------------------|-----------------------|
| <b>DIMM Density</b>                  | <b>32GB(2Rx8,x72)</b> |
| <b>Row address</b>                   | 64K A[15:0]           |
| <b>Column address</b>                | 1K A[9:0]             |
| <b>Device bank group address</b>     | 8 BG[2:0]             |
| <b>Device bank address per group</b> | 4 BA[1:0]             |
| <b>Device configuration</b>          | 16Gb(2Gx8)            |
| <b>Device Quantity</b>               | 20                    |

## 2 Pin Configurations

### 2.1 Pin Configurations

The pin configuration of the 288-Pin ECC UDIMM is listed by function in [Table 4](#) (288 pins).

**Table 4 - Pin Configuration ECC UDIMM (288 pin)**

| 288-Pin DDR5 UDIMM Front |          |     |          |     |          |     |          |
|--------------------------|----------|-----|----------|-----|----------|-----|----------|
| Pin                      | Symbol   | Pin | Symbol   | Pin | Symbol   | Pin | Symbol   |
| 1                        | VIN_BULK | 37  | DQ20_A   | 73  | CK0_A_c  | 109 | Vss      |
| 2                        | RFU      | 38  | Vss      | 74  | Vss      | 110 | DQ5_B    |
| 3                        | RFU      | 39  | DQ21_A   | 75  | RFU      | 111 | Vss      |
| 4                        | HSCL     | 40  | Vss      | 76  | RFU      | 112 | DQ8_B    |
| 5                        | HSDA     | 41  | DQ24_A   | 77  | Vss      | 113 | Vss      |
| 6                        | Vss      | 42  | Vss      | 78  | CK0_B_t  | 114 | DQ9_B    |
| 7                        | RFU      | 43  | DQ25_A   | 79  | CK0_B_c  | 115 | Vss      |
| 8                        | Vss      | 44  | Vss      | 80  | Vss      | 116 | DM1_B_n  |
| 9                        | DQ0_A    | 45  | DM3_A_n  | 81  | RFU      | 117 | Vss      |
| 10                       | Vss      | 46  | Vss      | 82  | CA12_B   | 118 | DQ12_B   |
| 11                       | DQ1_A    | 47  | DQ28_A   | 83  | Vss      | 119 | Vss      |
| 12                       | Vss      | 48  | Vss      | 84  | CA10_B   | 120 | DQ13_B   |
| 13                       | DQS0_A   | 49  | DQ29_A   | 85  | CA8_B    | 121 | Vss      |
| 14                       | DQS0_A_t | 50  | Vss      | 86  | Vss      | 122 | DQ16_B   |
| 15                       | Vss      | 51  | CB0_A    | 87  | CA6_B    | 123 | Vss      |
| 16                       | DQ4_A    | 52  | Vss      | 88  | CA4_B    | 124 | DQ17_B   |
| 17                       | Vss      | 53  | CB1_A    | 89  | Vss      | 125 | Vss      |
| 18                       | DQ5_A    | 54  | Vss      | 90  | CA2_B    | 126 | DQS2_B_c |
| 19                       | Vss      | 55  | DQS4_A_c | 91  | CA0_B    | 127 | DQS2_B_t |
| 20                       | DQ8_A    | 56  | DQS4_A_t | 92  | Vss      | 128 | Vss      |
| 21                       | Vss      | 57  | Vss      | 93  | Cs0_B_n  | 129 | DQ20_B   |
| 22                       | DQ9_A    | 58  | Cs0_A_n  | 94  | Vss      | 130 | Vss      |
| 23                       | Vss      | 59  | Vss      | 95  | RESET_n  | 131 | DQ21_B   |
| 24                       | DM1_A_n  | 60  | CA0_A    | 96  | Vss      | 132 | Vss      |
| 25                       | Vss      | 61  | CA2_A    | 97  | CB0_B    | 133 | DQ24_B   |
| 26                       | DQ12_A   | 62  | Vss      | 98  | Vss      | 134 | Vss      |
| 27                       | Vss      | 63  | CA4_A    | 99  | CB1_B    | 135 | DQ25_B   |
| 28                       | DQ13_A   | 64  | CA6_A    | 100 | Vss      | 136 | Vss      |
| 29                       | Vss      | 65  | Vss      | 101 | DQ0_B    | 137 | DM3_B_n  |
| 30                       | DQ16_A   | 66  | CA8_A    | 102 | Vss      | 138 | Vss      |
| 31                       | Vss      | 67  | CA10_A   | 103 | DQ1_B    | 139 | DQ28_B   |
| 32                       | DQ17_A   | 68  | Vss      | 104 | Vss      | 140 | Vss      |
| 33                       | Vss      | 69  | CA12_A   | 105 | DQS0_B_c | 141 | DQ29_B   |
| 34                       | DQS2_A_c | 70  | RFU      | 106 | DQS0_B_t | 142 | Vss      |
| 35                       | DQS2_A_t | 71  | Vss      | 107 | Vss      | 143 | RFU      |
| 36                       | Vss      | 72  | CK0_A_t  | 108 | DQ4_B    | 144 | RFU      |

| 288-Pin DDR5 UDIMM Back |          |     |          |     |          |     |          |
|-------------------------|----------|-----|----------|-----|----------|-----|----------|
| Pin                     | Symbol   | Pin | Symbol   | Pin | Symbol   | Pin | Symbol   |
| 145                     | VIN_BULK | 181 | DQ22_A   | 217 | CK1_A_c  | 253 | Vss      |
| 146                     | VIN_BULK | 182 | Vss      | 218 | Vss      | 254 | DQ7_B    |
| 147                     | PWR_GOOD | 183 | DQ23_A   | 219 | RFU      | 255 | Vss      |
| 148                     | HsA      | 184 | Vss      | 220 | RFU      | 256 | DQ10_B   |
| 149                     | RFU      | 185 | DQ26_A   | 221 | Vss      | 257 | Vss      |
| 150                     | Vss      | 186 | Vss      | 222 | CK1_B_t  | 258 | DQ11_B   |
| 151                     | PWR_EN   | 187 | DQ27_A   | 223 | CK1_B_c  | 259 | Vss      |
| 152                     | RFU      | 188 | Vss      | 224 | Vss      | 260 | DQS1_B_c |
| 153                     | Vss      | 189 | DQS3_A_c | 225 | RFU      | 261 | DQS1_B_t |
| 154                     | DQ2_A    | 190 | DQS3_A_t | 226 | RFU      | 262 | Vss      |
| 155                     | Vss      | 191 | Vss      | 227 | Vss      | 263 | DQ14_B   |
| 156                     | DQ3_A    | 192 | DQ30_A   | 228 | CA11_B   | 264 | Vss      |
| 157                     | Vss      | 193 | Vss      | 229 | CA9_B    | 265 | DQ15_B   |
| 158                     | DM0_A_n  | 194 | DQ31_A   | 230 | Vss      | 266 | Vss      |
| 159                     | Vss      | 195 | Vss      | 231 | CA7_B    | 267 | DQ18_B   |
| 160                     | DQ6_A    | 196 | CB2_A    | 232 | CA5_B    | 268 | Vss      |
| 161                     | Vss      | 197 | Vss      | 233 | Vss      | 269 | DQ19_B   |
| 162                     | DQ7_A    | 198 | CB3_A    | 234 | CA3_B    | 270 | Vss      |
| 163                     | Vss      | 199 | Vss      | 235 | CA1_B    | 271 | DM2_B_n  |
| 164                     | DQ10_A   | 200 | ALERT_n  | 236 | Vss      | 272 | Vss      |
| 165                     | Vss      | 201 | Vss      | 237 | CS1_B_n  | 273 | DQ22_B   |
| 166                     | DQ11_A   | 202 | CS1_A_n  | 238 | Vss      | 274 | Vss      |
| 167                     | Vss      | 203 | Vss      | 239 | DQS4_B_c | 275 | DQ23_B   |
| 168                     | DQS1_A_c | 204 | CA1_A    | 240 | DQS4_B_t | 276 | Vss      |
| 169                     | DQS1_A_t | 205 | CA3_A    | 241 | Vss      | 277 | DQ26_B   |
| 170                     | Vss      | 206 | Vss      | 242 | CB2_B    | 278 | Vss      |
| 171                     | DQ14_A   | 207 | CA5_A    | 243 | Vss      | 279 | DQ27_B   |
| 172                     | Vss      | 208 | CA7_A    | 244 | CB3_B    | 280 | Vss      |
| 173                     | DQ15_A   | 209 | Vss      | 245 | Vss      | 281 | DQS3_B_c |
| 174                     | Vss      | 210 | CA9_A    | 246 | DQ2_B    | 282 | DQS3_B_t |
| 175                     | DQ18_A   | 211 | CA11_A   | 247 | Vss      | 283 | Vss      |
| 176                     | Vss      | 212 | Vss      | 248 | DQ3_B    | 284 | DQ30_B   |
| 177                     | DQ19_A   | 213 | RFU      | 249 | Vss      | 285 | Vss      |
| 178                     | Vss      | 214 | RFU      | 250 | DM0_B_n  | 286 | DQ31_B   |
| 179                     | DM2_A_n  | 215 | Vss      | 251 | Vss      | 287 | Vss      |
| 180                     | Vss      | 216 | CK1_A_t  | 252 | DQ6_B    | 288 | RFU      |

## 2.2 Pin Descriptions

Table 5 - Pin Descriptions

| Symbol                                                   | Type         | I/O Level | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
|----------------------------------------------------------|--------------|-----------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| CK[1:0]_A_t<br>CK[1:0]_B_t<br>CK[1:0]_A_c<br>CK[1:0]_B_c | Input        | VDDQ      | Clock: CK_t and CK_c are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK_t and negative edge of CK_c.                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| CA[12:0]_A<br>CA[12:0]_B                                 | DDR Input    | VDDQ      | Command/Address Inputs: CA signals provide the command and address inputs according to the Command Truth Table. Note: Since some commands are multi-cycle, the pins may not be interchanged between devices on the same bus. The address inputs also provide the op-code during MODE REGISTER SET commands.                                                                                                                                                                                                                                                                                                                                        |
| CS[1:0]_A<br>CS[1:0]_B                                   | Input        | VDDQ      | Chip Select: All commands are masked when CS_n is registered HIGH. CS_n provides for external rank selection on systems with multiple ranks. CS_n is considered part of the command code. CS_n is also used to enter and exit the parts from power down mode and self refresh mode. While not in self refresh mode the CS_n input buffer operates with the same ODT and VREF parameters as configured by the CA_ODT strap setting or mode register. When in self refresh, the CS_n is a CMOS rail-to-rail signal with DC HIGH and LOW at 80% and 20% of VDD.                                                                                       |
| ALERT_n                                                  | Output       | VDDQ      | Alert: If there is an error in CRC, then ALERT_n drives LOW for the period time interval and returns HIGH. During connectivity test mode, this pin functions as an input. Usage of this signal is system-dependent. In the case where this pin is not connected, ALERT_n must be bonded to VDDQ on the system board.                                                                                                                                                                                                                                                                                                                               |
| RESET_n                                                  | CMOS Input   | VDDQ      | Active Low Asynchronous Reset: Reset is active when RESET_n is LOW, and inactive when RESET_n is HIGH. RESET_n must be HIGH during normal operation. RESET_n is a CMOS rail-to-rail signal with DC HIGH and LOW at 80% and 20% of VDDQ.                                                                                                                                                                                                                                                                                                                                                                                                            |
| Power_Good                                               | Input/Output | VDDQ      | Power Good Indicator: Open drain output. The PMIC ensures this pin HIGH when VIN_Bulk input supply, as well as all enabled output buck regulators and all LDO regulators tolerance threshold is maintained as configured in the appropriate register. The PMIC drives this pin LOW when VIN_Bulk input goes below the threshold or when any of the enabled output buck regulator exceeds the thresholds configured in the appropriate register or when any LDO output regulator exceeds the threshold configured in the appropriate register. As an input, the PMIC disables its output regulator when this pin is LOW. The LDO outputs remain on. |
| HSCL                                                     | Input        | VOUT_1.0V | Host Sideband Bus Clock: Bus clock used to strobe data into HUB device. When open drain, a pull-up resistor is required on the system motherboard.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| HSDA                                                     | Input/Output | VOUT_1.0V | Host Sideband Bus Data: I2C/I3C-Basic data. When open drain, a pull-up resistor is required on the system motherboard.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| HSA                                                      | Input        | GND       | Host Sideband Bus Device ID: Address input to a hub or other client device to distinguish between identical devices in the I3C basic address range. Tied to GND, HSA has different resistor values on the motherboard to identify DIMM slot address. Refer to the SPD Hub spec for more information.                                                                                                                                                                                                                                                                                                                                               |

| Symbol                                                           | Type         | I/O Level | Description                                                                                                                                                                                                                                                                                                                                                              |
|------------------------------------------------------------------|--------------|-----------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| DQ[31:0]_A<br>DQ[31:0]_B                                         | Input/Output | VDDQ      | Data Input/Output: Bidirectional data bus. If CRC is enabled via the mode register, then CRC code is added at the end of data burst. Any DQ from DQ0—DQ3 may indicate the internal VREF level during test via mode register setting MR4 A4 = HIGH. Refer to the vendor-specific data sheets to determine which DQ is used.                                               |
| CB[7:0]_A<br>CB[7:0]_B                                           | Input/Output | VDDQ      | ECC Check Bits Input/Output: Bidirectional data bus on UDIMM With ECC                                                                                                                                                                                                                                                                                                    |
| DQS[4:0]_A_t<br>DQS[4:0]_B_t<br><br>DQS[4:0]_A_c<br>DQS[4:0]_B_c | Input/Output | VDDQ      | Data Strobe: Output with read data, input with write data. Edge-aligned with read data, centered in write data. The data strobe DQS_t is paired with differential signals DQS_c, respectively, to provide differential pair signaling to the system during reads and writes. DDR5 SDRAM only supports differential data strobe. It does not support single-ended strobe. |
| DM[3:0]_A_n<br>DM[3:0]_B_n                                       | Input        | VDDQ      | Input Data Mask: DM_n is an input mask signal for write data. Input data is masked when DM_n is sampled LOW coincident with that input data during a write access. DM_n is sampled on both edges of DQS. For x8 device, the function of DM_n is enabled by MR5:OP[5] = 1.                                                                                                |
| PWR_EN                                                           | Input        | 3.3V      | PMIC Enable. When this pin is high, the PMIC turns on the regulator. When this pin is low, the PMIC turns off the regulator. This signal is connected to PMIC's VR_EN pin.                                                                                                                                                                                               |
| VIN_BULK                                                         | Supply       |           | External Power Supply: 5V, 4.25V (min), 5.5V (max)                                                                                                                                                                                                                                                                                                                       |
| VSS                                                              | Supply       |           | Ground                                                                                                                                                                                                                                                                                                                                                                   |
| RFU                                                              |              |           | Reserved for future use. No on DIMM electrical connection is present.                                                                                                                                                                                                                                                                                                    |
| NC                                                               |              |           | No connect: No internal electrical connection is present.                                                                                                                                                                                                                                                                                                                |
| NF                                                               |              |           | No function: May have internal connection present, but has no function.                                                                                                                                                                                                                                                                                                  |

## 3 General Description

### 3.1 General Description

High-speed DDR5 SDRAM modules use DDR5 SDRAM devices with four or eight internal memory bank groups. DDR5 SDRAM modules benefit from DDR5 SDRAM's use of a 16n-prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single READ or WRITE operation for the DDR5 SDRAM effectively consists of a single 16n-bit-wide, eight-clock data transfer at the internal DRAM core and sixteen corresponding n-bit-wide, one-half-clock-cycle data transfers at the I/O pins.

DDR5 modules use two sets of differential signals (DQS\_t and DQS\_c) to capture data, and CK\_t and CK\_c to capture commands, addresses, and control signals. Differential clocks and data strobes ensure exceptional noise immunity for these signals and provide precise crossing points to capture input signals.

## 3.2 Power Management Integrated Circuit Operation

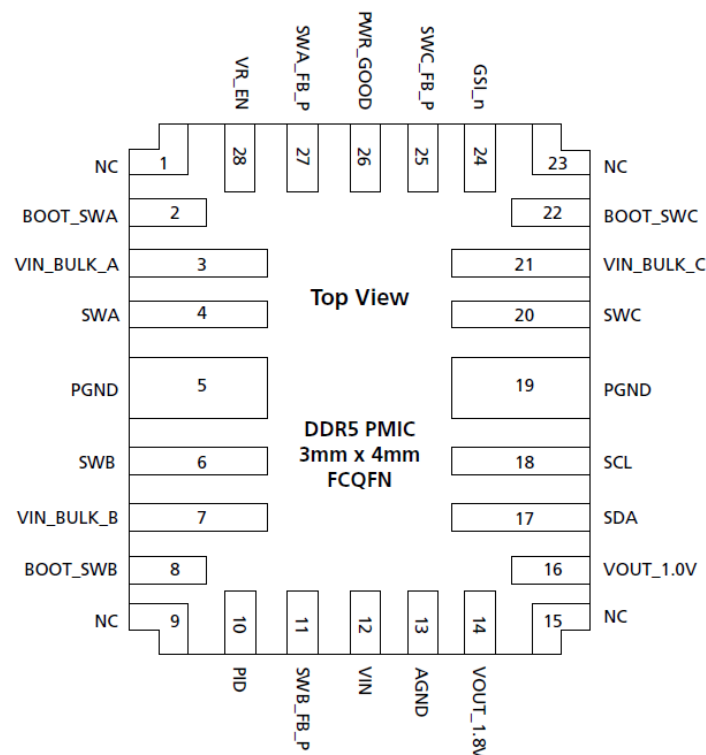
The power management integrated circuit (PMIC) is new for DDR5. For UDIMMs, JEDEC defines PMIC5100. This operation converts a 5V supply into regulated values for components on the module. The PMIC allows the host to monitor voltage and current via the sideband channel.

The PMIC5100 has one 5V nominal supply input pin from the card edge through VIN\_Bulk. The PMIC has the ability to regulate lower voltages to the HUB which allows external access to read/configure this device prior to the VR ENABLE command. The VIN\_Bulk supply, after the VR ENABLE command, will supply all regulated voltages to the PMIC and DRAM.

By default, the PMIC powers up in I2C mode, and the host can reconfigure to support I3C-basic if needed. Please see the address configuration as below table for the PMIC Address ID (PID), device pin #10.

**Table 6 - PMIC Addressing**

| PID Configuration (Pin #10) | PMIC Address ID ( PID ) |       |       |       |
|-----------------------------|-------------------------|-------|-------|-------|
|                             | Bit 7                   | Bit 6 | Bit 5 | Bit 4 |
| Pin to Vss                  | 1                       | 0     | 0     | 1     |



### 3.3 SPD EEPROM HUB Operation

DDR5 SDRAM modules incorporate an SPD EEPROM with hub function with integrated thermal sensor (TS). The SPD data is stored in a 1024-byte including 16 blocks (64 bytes per block), and each block may optionally be write-protected via software command.

The EEPROM resides on a two-wire I3C serial interface, which is also compatible with legacy I2C interface and is not integrated with the memory bus in any manner. It operates as an initiator/target device in the I3C-basic protocol, with all operations synchronized by the serial clock. Transfer rates of up to 12.5 MHz are achievable at 1.0V (NOM).

The first 640 bytes are programmed by UnilC for DIMM parameters related usage. The remaining 384 bytes are available for the end user.

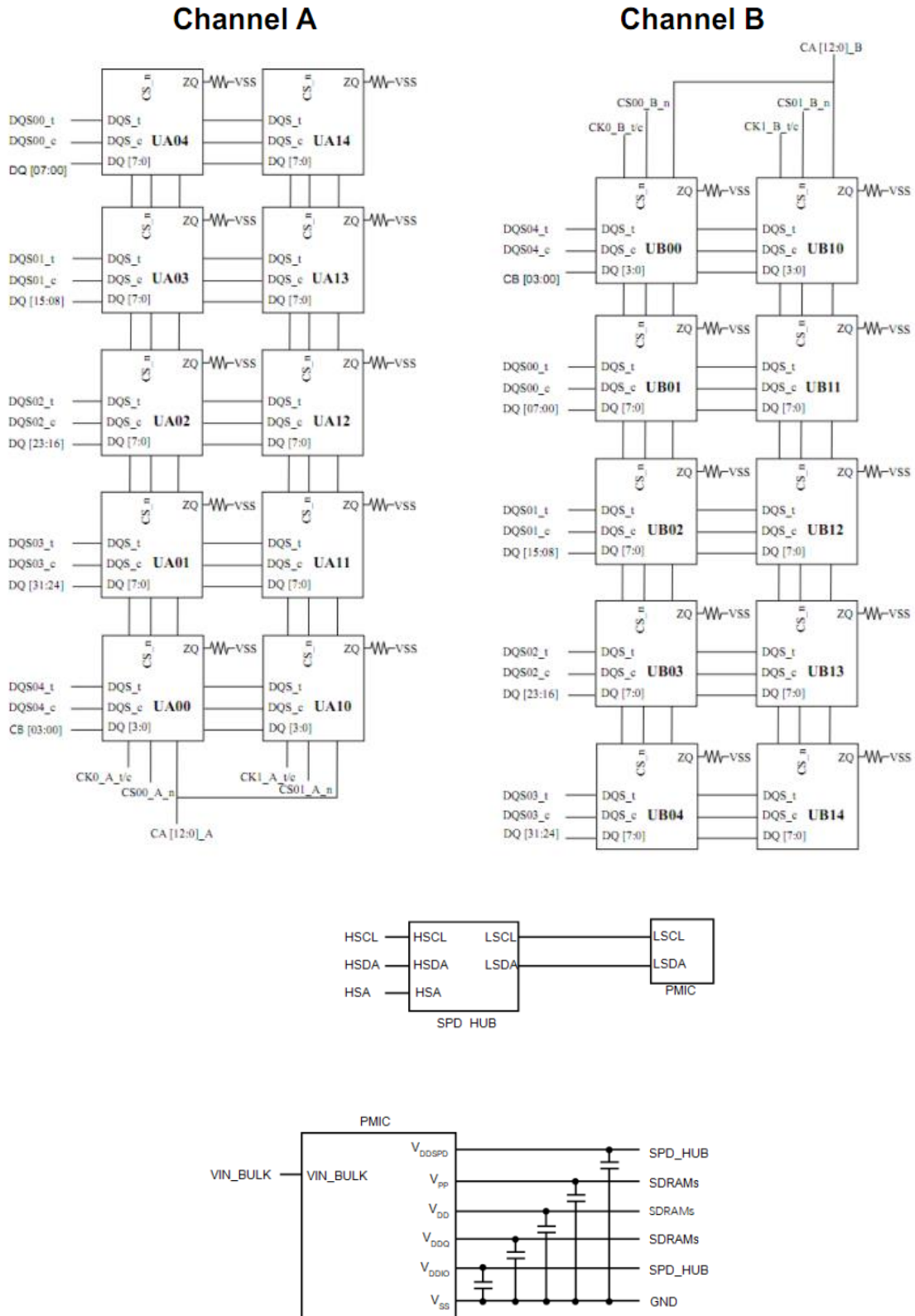
UnilC implements reversible software write protection on DDR5 SDRAM-based modules. This prevents the lower 640 bytes (bytes 0 to 639) from being inadvertently programmed or corrupted. The upper 384 bytes remain available for customer use and are unprotected.

**Table 7 - SPD Byte Information**

| Block | Range    |             | Description                                               |
|-------|----------|-------------|-----------------------------------------------------------|
| 0     | 0~63     | 0x000~0x03F | Base configuration and DRAM parameters                    |
| 1     | 64~127   | 0x040~0x07F | Base configuration and DRAM parameters                    |
| 2     | 128~191  | 0x080~0x0BF | Reserved for future use                                   |
| 3     | 192~239  | 0x0C0~0x0EF | Common Module Parameters -- See annex A.0 for details     |
|       | 240~255  | 0x0D0~0x0FF | Standard module parameters -- See annexes A.x for details |
| 4     | 256~319  | 0x100~0x13F | Standard module parameters -- See annexes A.x for details |
| 5     | 320~383  | 0x140~0x17F | Standard module parameters -- See annexes A.x for details |
| 6     | 384~447  | 0x180~0x1BF | Standard module parameters -- See annexes A.x for details |
| 7     | 448~509  | 0x1C0~0x1FF | Reserved for future use                                   |
|       | 510~511  | 0x1FE~0x1FF | CRC for SPD bytes 0~509                                   |
| 8     | 512~575  | 0x200~0x23F | Manufacturing information                                 |
| 9     | 576~639  | 0x240~0x27F | Manufacturing information                                 |
| 10    | 640~703  | 0x280~0x2BF | End user programmable                                     |
| 11    | 704~767  | 0x2C0~0x2FF | End user programmable                                     |
| 12    | 768~831  | 0x300~0x33F | End user programmable                                     |
| 13    | 832~895  | 0x340~0x37F | End user programmable                                     |
| 14    | 896~959  | 0x380~0x3BF | End user programmable                                     |
| 15    | 960~1023 | 0x3C0~0x3FF | End user programmable                                     |

## 3.4 Function Block Diagram

Figure 1 - Function Block Diagram\_SCA32GE13H1F1C-56B



## 3.5 DQ Map

Table 8 - DQ Map \_SCA32GE13H1F1C-56B

| Module Pin NO. | Module DQ NO. | R0 IC NO. | R0 IC DQ | R1 IC NO. | R1 IC DQ | Module Pin NO. | Module DQ NO. | R0 IC NO. | R0 IC DQ | R1 IC NO. | R1 IC DQ |
|----------------|---------------|-----------|----------|-----------|----------|----------------|---------------|-----------|----------|-----------|----------|
| 9              | 0_A           | UA04      | 3        | UA14      | 2        | 20             | 8_A           | UA03      | 1        | UA13      | 0        |
| 11             | 1_A           |           | 2        |           | 3        | 22             | 9_A           |           | 3        |           | 2        |
| 154            | 2_A           |           | 1        |           | 0        | 164            | 10_A          |           | 2        |           | 3        |
| 156            | 3_A           |           | 0        |           | 1        | 166            | 11_A          |           | 0        |           | 1        |
| 16             | 4_A           |           | 5        |           | 4        | 26             | 12_A          |           | 5        |           | 4        |
| 18             | 5_A           |           | 6        |           | 7        | 28             | 13_A          |           | 6        |           | 7        |
| 160            | 6_A           |           | 7        |           | 6        | 171            | 14_A          |           | 7        |           | 6        |
| 162            | 7_A           |           | 4        |           | 5        | 173            | 15_A          |           | 4        |           | 5        |
| 30             | 16_A          | UA02      | 5        | UA12      | 4        | 41             | 24_A          | UA01      | 5        | UA11      | 4        |
| 32             | 17_A          |           | 7        |           | 6        | 43             | 25_A          |           | 6        |           | 7        |
| 175            | 18_A          |           | 6        |           | 7        | 185            | 26_A          |           | 7        |           | 6        |
| 177            | 19_A          |           | 4        |           | 5        | 187            | 27_A          |           | 4        |           | 5        |
| 37             | 20_A          |           | 1        |           | 0        | 47             | 28_A          |           | 1        |           | 0        |
| 39             | 21_A          |           | 3        |           | 2        | 49             | 29_A          |           | 0        |           | 1        |
| 181            | 22_A          |           | 2        |           | 3        | 192            | 30_A          |           | 3        |           | 2        |
| 183            | 23_A          |           | 0        |           | 1        | 194            | 31_A          |           | 2        |           | 3        |
| 51             | CB00_A        | UA00      | 1        | UA10      | 0        | 97             | CB00_B        | UB00      | 1        | UB10      | 0        |
| 53             | CB01_A        |           | 3        |           | 2        | 99             | CB01_B        |           | 0        |           | 1        |
| 196            | CB02_A        |           | 2        |           | 3        | 242            | CB02_B        |           | 3        |           | 2        |
| 198            | CB03_A        |           | 0        |           | 1        | 244            | CB03_B        |           | 2        |           | 3        |
| 101            | 0_B           | UB01      | 1        | UB11      | 0        | 112            | 8_B           | UB02      | 1        | UB12      | 0        |
| 103            | 1_B           |           | 3        |           | 2        | 114            | 9_B           |           | 3        |           | 2        |
| 246            | 2_B           |           | 2        |           | 3        | 256            | 10_B          |           | 0        |           | 1        |
| 248            | 3_B           |           | 0        |           | 1        | 258            | 11_B          |           | 2        |           | 3        |
| 108            | 4_B           |           | 5        |           | 4        | 118            | 12_B          |           | 5        |           | 4        |
| 110            | 5_B           |           | 6        |           | 7        | 120            | 13_B          |           | 6        |           | 7        |
| 252            | 6_B           |           | 7        |           | 6        | 263            | 14_B          |           | 7        |           | 6        |
| 254            | 7_B           |           | 4        |           | 5        | 265            | 15_B          |           | 4        |           | 5        |
| 122            | 16_B          | UB03      | 3        | UB13      | 2        | 133            | 24_B          | UB04      | 5        | UB14      | 4        |
| 124            | 17_B          |           | 1        |           | 0        | 135            | 25_B          |           | 7        |           | 6        |
| 267            | 18_B          |           | 0        |           | 1        | 277            | 26_B          |           | 6        |           | 7        |
| 269            | 19_B          |           | 2        |           | 3        | 279            | 27_B          |           | 4        |           | 5        |
| 129            | 20_B          |           | 5        |           | 4        | 139            | 28_B          |           | 1        |           | 0        |
| 131            | 21_B          |           | 6        |           | 7        | 141            | 29_B          |           | 0        |           | 1        |
| 273            | 22_B          |           | 7        |           | 6        | 284            | 30_B          |           | 3        |           | 2        |
| 275            | 23_B          |           | 4        |           | 5        | 286            | 31_B          |           | 2        |           | 3        |

## 4 Electrical Characteristics

### 4.1 AC and DC Operation Conditions

**Table 9 - Absolute Maximum DC Ratings**

| Symbol            | Parameter                                     | Rating |      | Unit | Note  |
|-------------------|-----------------------------------------------|--------|------|------|-------|
|                   |                                               | Min.   | Max. |      |       |
| $V_{DD}$          | Voltage on $V_{DD}$ pin relative to $V_{SS}$  | -0.3   | +1.4 | V    | 1)    |
| $V_{DDQ}$         | Voltage on $V_{DDQ}$ pin relative to $V_{SS}$ | -0.3   | +1.4 | V    | 1)    |
| $V_{PP}$          | Voltage on $V_{PP}$ pin relative to $V_{SS}$  | -0.3   | +2.1 | V    | 3)    |
| $V_{IN}, V_{OUT}$ | Voltage on any pin relative to $V_{SS}$       | -0.3   | +1.4 | V    | 1)    |
| $T_{STG}$         | Storage Temperature                           | -55    | +100 | °C   | 1),2) |

Notes:

- 1) Stresses greater than those listed in this table may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- 2) Storage temperature is the case surface temperature on the center/top side of the device. For the measurement conditions, refer to JESD51-2 standard.
- 3)  $V_{PP}$  must be equal or greater than  $V_{DD} / V_{DDQ}$  at all times during power on and operation of DRAM device.

**Table 10 - DC Voltage Operating Conditions**

| Symbol    | Parameter                                     | Low Frequency Voltage Spec |     |            | Unit | Note   |
|-----------|-----------------------------------------------|----------------------------|-----|------------|------|--------|
|           |                                               | Min.                       | Typ | Max.       |      |        |
| $V_{DD}$  | Voltage on $V_{DD}$ pin relative to $V_{SS}$  | 1.067(-3%)                 | 1.1 | 1.166(+6%) | V    | 1), 2) |
| $V_{DDQ}$ | Voltage on $V_{DDQ}$ pin relative to $V_{SS}$ | 1.067(-3%)                 | 1.1 | 1.166(+6%) | V    | 1), 2) |
| $V_{PP}$  | Voltage on $V_{PP}$ pin relative to $V_{SS}$  | 1.746(-3%)                 | 1.8 | 1.908(+6%) | V    | 1), 2) |

Notes:

- 1)  $V_{DD}$  must be within 66mV of  $V_{DDQ}$ .
- 2) AC parameters are measured with  $V_{DD}$  and  $V_{DDQ}$  tied together.

**Table 11 - DRAM Component Operating Temperature Range**

| Symbol                      | Parameter                      | Rating |      | Unit | Grade | Note        |
|-----------------------------|--------------------------------|--------|------|------|-------|-------------|
|                             |                                | Min.   | Max. |      |       |             |
| $T_{\text{OPER\_NORMAL}}$   | Normal Operating Temperature   | 0      | 85   | °C   | NT    | 1),2),3),4) |
| $T_{\text{OPER\_EXTENDED}}$ | Extended Operating Temperature | 0      | 95   | °C   | XT    | 1),2),3),4) |

Notes:

- 1) All operating temperature symbols, ranges, acronyms from JESD402-1.
- 2) Operating Temperature is the case surface temperature on the center / top side of the DRAM. For the measurement conditions, refer to JESD51-2.
- 3) All devices are required to operate in NT and XT temperature ranges.
- 4) When operating above 85°C , the host shall provide appropriate refresh mode controls associated with increased temperature range. The full description of these settings are defined in the tREFI parameters for REFab and REFsb command by device density table in the Refresh operations section (DRAM datasheet).

## 4.2 Module and Component Speed Grades

DDR5 components may exceed the listed module speed grades; module may not be available in all listed speed grades

**Table 12 - Module and Component Speed Grades**

| Module Speed Grade | Component Speed Grade |
|--------------------|-----------------------|
| -56B               | 5600-46-45-45         |

## 4.3 I<sub>DD</sub> Specifications

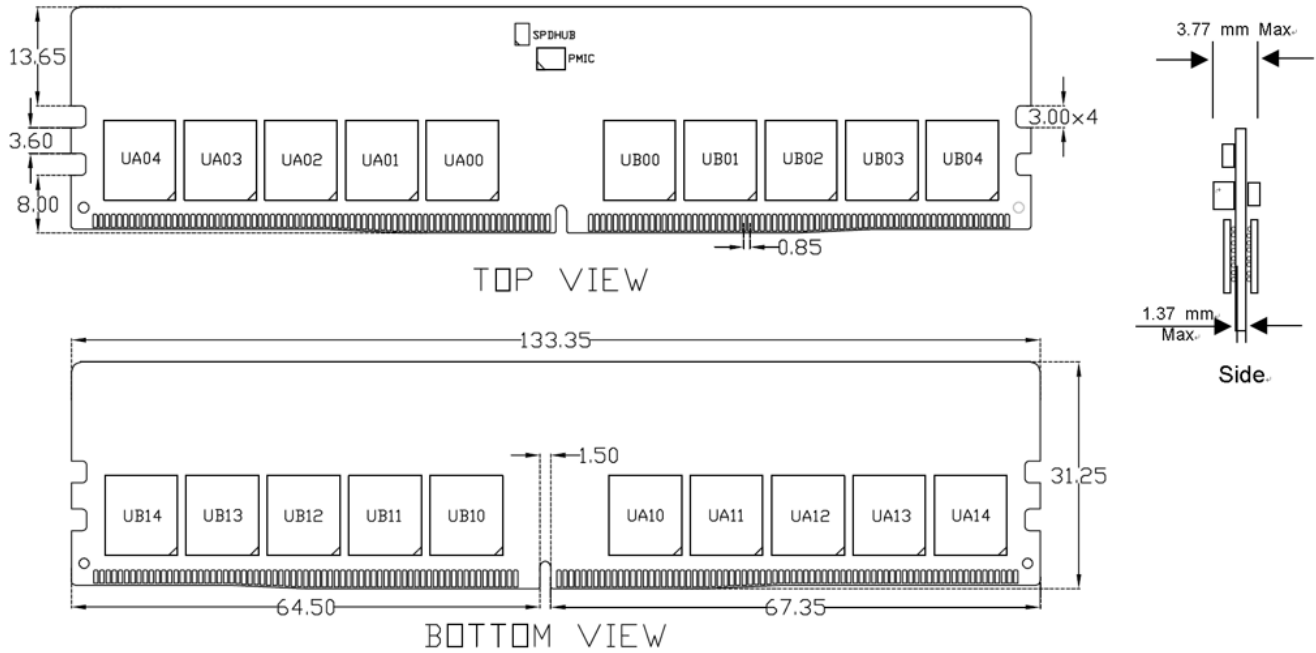
**Table 13 - I<sub>DD</sub> Specification for SCA32GE13H1F1C-56B**

Module IDD is based on PMIC VIN\_BULK 5V input current and typical operating temperature. Each IDD parameter includes PMIC efficiency and all DRAM current on all supplies (VDD, VDDQ and VPP).

| Product Type                                          |        | SCA32GE13H1F1C-56B | Unit | Note |
|-------------------------------------------------------|--------|--------------------|------|------|
| Organization                                          |        | 32GB               |      |      |
|                                                       |        | 2Rank (×8)         |      |      |
|                                                       |        | ×72                |      |      |
|                                                       |        | -56B               |      |      |
| Parameter                                             | Symbol | Current            |      |      |
| Operating one bank ACTIVATE-PRECHARGE current         | IDD0   | 336.1              | mA   |      |
| Operating four bank ACTIVATE-PRECHARGE current        | IDD0F  | 443.5              | mA   |      |
| Precharge standby current                             | IDD2N  | 295.8              | mA   |      |
| Precharge power-down current                          | IDD2P  | 266.2              | mA   |      |
| Active standby current                                | IDD3N  | 445.5              | mA   |      |
| Active power-down current                             | IDD3P  | 414.9              | mA   |      |
| Operating burst read current                          | IDD4R  | 1040.9             | mA   |      |
| Operating burst write current                         | IDD4W  | 1239.3             | mA   |      |
| Burst refresh (normal refresh mode) current           | IDD5B  | 865.8              | mA   |      |
| Burst refresh (fine granularity refresh mode) current | IDD5F  | 827.9              | mA   |      |
| Burst refresh (same bank refresh mode) current        | IDD5C  | 531.5              | mA   |      |
| Self refresh current                                  | IDD6N  | 293.5              | mA   |      |
| Operating bank interleave read current                | IDD7   | 1300.5             | mA   |      |
| Maximum power saving deep power down mode current     | IDD8   | 130.5              | mA   |      |

## 5 Package Dimensions

Figure 2 - Package Dimensions\_SCA32GE13H1F1C-56B



Note: 1. All dimensions are in millimeters.  
2. The dimensional diagram is for reference only.

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