May. 2022

SCC08GE03C2F1V-32AA

288-Pin DDR4 VLP ECC Unbuffered DIMM (X72, ECC)
EU RoHS Compliant

Data Sheet

Rev. A

Revision History		
Date	**Revision**	**Subjects (major changes since last revision)**
2022-05	A	Initial Release

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Contents

1 Overview

This chapter gives an overview of the 288-pin DDR4 VLP ECC UDIMM product family and describes its main characteristics.

1.1 Features

- 288-Pin PC4-3200 DDR4 VLP ECC UDIMM
- Frequency/CAS latency:
  0.625ns @ CL = 22 (DDR4-3200)
- VDD = 1.2V ±60mV
- VPP = 2.5V (2.375V~2.75V)
- VDDSPD = 2.5V
- Programmable CAS latency 9, 10,11, 12, 13, 14, 15
  16, 17, 18,19 20,21,22 and 24 supported
- Programmable additive latency 0, CL-1, and CL-2
  supported (x4/x8 only)
- Programmable CAS Write latency (CWL) = 9, 10, 11, 12,
  14, 16, 18, 20
- Programmable burst length 4/8 with both nibble
  sequential and interleave mode
- Data bus inversion (DBI) for data bus
- Fly-by topology
- Terminated control command and address bus
- BL switch on the fly
- 16 internal banks; 4 groups of 4 banks each
- Nominal and dynamic on-die termination (ODT)
  for strobe, and mask signals
- Low-power auto self refresh (LPASR)
- On-die VREFDQ generation and calibration
- Fixed burst chop (BC) of 4 and burst length (BL)
  of 8 via the mode register set (MRS)
- Gold edge contacts
- Halogen-free
- Average Refresh Cycle (Tcase of 0 °C ~ 95 °C)
  - 7.8 µs at 0 °C ~ 85 °C
  - 3.9 µs at 85 °C ~ 95 °C

Table 1 - Module Performance Table

UniIC Speed Code		**-32AA**	**Unit**	**Note**
DRAM Speed Grade	**DDR4**	**-3200**	**MT/s**	
CAS-RCD-RP latencies		**22-22-22**	t_{CK}	
Min. RAS-CAS-Delay	t_{RCD}	13.75	ns	
Min. Row Precharge Time	t_{RP}	13.75	ns	
Min. Row Active Time	t_{RAS}	32	ns	
Min. Row Cycle Time	t_{RC}	45.75	ns	

1.2 Description

The UniIC 8GB module family is DDR4 VLP ECC UDIMM with 18.75mm height based on DDR4 technology. DIMMs are intended for mounting into 288-pin connector sockets.

The memory array is designed with 8 Gbit Double-Data- Rate-Four (DDR4) Synchronous DRAMs. Decoupling capacitors are mounted on the PCB board. The DIMMs feature serial presence detects based on a serial E^2PROM device using the 2-pin I^2C protocol.

green Product

Table 2 - Ordering Information

Product Type[1)]	Compliance Code[2)]	Description	SDRAM Technology
PC4-3200 (22-22-22)			
SCC08GE03C2F1V-32AA	8GB 1R×8 PC4-3200-22-22-22	1Rank	8Gbit (×8)

1) For detailed information regarding Product Type of UniIC please see chapter "Product Type Nomenclature" of this data sheet.
2) The Compliance Code is printed on the module label and describes the speed grade, for example "PC4-3200-22-22-22" where 3200 means DIMM modules with 3200MHz data frequency and "22-22-22" means Column Address Strobe (CAS) latency=22, Row Column Delay (RCD) latency = 22 and Row Precharge (RP) latency = 22.

Table 3 - Address Format

DIMM Density	8GB(1Rx8,X72)
Row address	64K A[15:0]
Column address	1K A[9:0]
Device bank group address	4 BG[1:0]
Device bank address per group	4 BA[1:0]
Device configuration	8Gb(1Gx8)
Module rank address	1CS_n[0]
Device Quantity	9

2 Pin Configurations

2.1 Pin Configurations

The pin configuration of the 288-Pin DDR4 VLP ECC UDIMM is listed by function in **Table 4** (288 pins).

Table 4 - Pin Configuration VLP ECC UDIMM (288 pin)

Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	NC	145	NC	39	VSS	183	DQ25	77	VTT	221	VTT	114	VSS	258	DQ47
2	VSS	146	VREFCA	40	DM3_n, DBI3_n, NC	184	VSS	KEY				115	DQ42	259	VSS
3	DQ4	147	VSS	41	NC	185	DQS3_c	78	EVENT_n	222	PARITY	116	VSS	260	DQ43
4	VSS	148	DQ5	42	VSS	186	DQS3_t	79	A0	223	VDD	117	DQ52	261	VSS
5	DQ0	149	VSS	43	DQ30	187	VSS	80	VDD	224	BA1	118	VSS	262	DQ53
6	VSS	150	DQ1	44	VSS	188	DQ31	81	BA0	225	A10/AP	119	DQ48	263	VSS
7	DM0_n, DBI0_n, NC	151	VSS	45	DQ26	189	VSS	82	RAS_n /A16	226	VDD	120	VSS	264	DQ49
8	NC	152	DQS0_c	46	VSS	190	DQ27	83	VDD	227	RFU	121	DM6_n, DBI6_n, NC	265	VSS
9	VSS	153	DQS0_t	47	CB4	191	VSS	84	CS0_n	228	WE_n /A14	122	NC	266	DQS6_c
10	DQ6	154	VSS	48	VSS	192	CB5	85	VDD	229	VDD	123	VSS	267	DQS6_t
11	VSS	155	DQ7	49	CB0	193	VSS	86	CAS_n /A15	230	NC	124	DQ54	268	VSS
12	DQ2	156	VSS	50	VSS	194	CB1	87	ODT0	231	VDD	125	VSS	269	DQ55
13	VSS	157	DQ3	51	DM8_n, DBI8_n, NC	195	VSS	88	VDD	232	A13	126	DQ50	270	VSS
14	DQ12	158	VSS	52	NC	196	DQS8_c	89	CS1_n	233	VDD	127	VSS	271	DQ51
15	VSS	159	DQ13	53	VSS	197	DQS8_t	90	VDD	234	NC	128	DQ60	272	VSS
16	DQ8	160	VSS	54	CB6	198	VSS	91	ODT1	235	NC	129	VSS	273	DQ61
17	VSS	161	DQ9	55	VSS	199	CB7	92	VDD	236	VDD	130	DQ56	274	VSS
18	DM1_n, DBI1_n, NC	162	VSS	56	CB2	200	VSS	93	NC	237	NC	131	VSS	275	DQ57
19	NC	163	DQS1_c	57	VSS	201	CB3	94	VSS	238	SA2	132	DM7_n, DBI7_n, NC	276	VSS
20	VSS	164	DQS1_t	58	RESET_n	202	VSS	95	DQ36	239	VSS	133	NC	277	DQS7_c

Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
21	DQ14	165	VSS	59	VDD	203	CKE1	96	VSS	240	DQ37	134	VSS	278	DQS7_t
22	VSS	166	DQ15	60	CKE0	204	VDD	97	DQ32	241	VSS	135	DQ62	279	VSS
23	DQ10	167	VSS	61	VDD	205	RFU	98	VSS	242	DQ33	136	VSS	280	DQ63
24	VSS	168	DQ11	62	ACT_n	206	VDD	99	DM4_n, DBI4_n, NC	243	VSS	137	DQ58	281	VSS
25	DQ20	169	VSS	63	BG0	207	BG1	100	NC	244	DQS4_c	138	VSS	282	DQ59
26	VSS	170	DQ21	64	VDD	208	ALERT_n	101	VSS	245	DQS4_t	139	SA0	283	VSS
27	DQ16	171	VSS	65	A12 /BC_n	209	VDD	102	DQ38	246	VSS	140	SA1	284	VDDSPD
28	VSS	172	DQ17	66	A9	210	A11	103	VSS	247	DQ39	141	SCL	285	SDA
29	DM2_n, DBI2_n, NC	173	VSS	67	VDD	211	A7	104	DQ34	248	VSS	142	VPP	286	VPP
30	NC	174	DQS2_c	68	A8	212	VDD	105	VSS	249	DQ35	143	VPP	287	VPP
31	VSS	175	DQS2_t	69	A6	213	A5	106	DQ44	250	VSS	144	RFU	288	VPP
32	DQ22	176	VSS	70	VDD	214	A4	107	VSS	251	DQ45				
33	VSS	177	DQ23	71	A3	215	VDD	108	DQ40	252	VSS				
34	DQ18	178	VSS	72	A1	216	A2	109	VSS	253	DQ41				
35	VSS	179	DQ19	73	VDD	217	VDD	110	DM5_n, DBI5_n, NC	254	VSS				
36	DQ28	180	VSS	74	CK0_t	218	CK1_t	111	NC	255	DQS5_c				
37	VSS	181	DQ29	75	CK0_c	219	CK1_c	112	VSS	256	DQS5_t				
38	DQ24	182	VSS	76	VDD	220	VDD	113	DQ46	257	VSS				

2.2 Pin Descriptions

Table 5 - Pin Descriptions

Symbol	Type	Function
CKx_t, CKx_c,	Input	Clock: CK_t and CK_c are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK_t and negative edge of CK_c.
CKEx	Input	Clock Enable: CKE HIGH activates and CKE LOW deactivates internal clock signals and device input buffers and output drivers. Taking CKE LOW provides Precharge Power-Down and Self-Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is synchronous for Self-Refresh exit. After VREFCA and Internal DQ Vref have become stable during the power on and initialization sequence, they must be maintained during all operations (including Self-Refresh). CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK_t, CK_c, ODT and CKE, are disabled during power-down. Input buffers, excluding CKE, are disabled during Self-Refresh.
CSx_n	Input	Chip Select: All commands are masked when CS-n is registered HIGH. CS_n provides for external Rank selection. CS_n is considered part of the command code.
Cx	Input	Chip ID : Chip ID is only used for 3DS for 2,4,8 high stack via TSV to select each slice of stacked component. Chip ID is considered part of the command code.
ODTx	Input	On Die Termination: ODT (registered HIGH) enables RTT_NOM termination resistance internal to the DDR4 SDRAM. When enabled, ODT is only applied to each DQ, DQS_t, DQS_c, TDQS_t and TDQS_c signal. The ODT pin will be ignored if MR1 is programmed to disable RTT_NOM.
ACT_n	Input	Activation Command Input: ACT_n defines the Activation command being entered along with CS_n. The input into RAS_n/A16, CAS_n/A15 and WE_n/A14 will be considered as Row Address A16, A15 and A14
RAS_n/A16. CAS_n/A15. WE_n/A14	Input	Command Inputs: RAS_n/A16, CAS_n/A15 and WE_n/A14 (along with CS_n) define the command being entered. Those pins have multi function. For example, for activation with ACT_n Low, these are Addresses like A16, A15 and A14 but for non-activation command with ACT_n High, these are Command pins for Read, Write and other command defined in command truth table
BGx	Input	Bank Group Inputs: BG0 - BG1 define which bank group an Active, Read, Write or Precharge command is being applied. BG0 also determines which mode register is to be accessed during a MRS cycle.
BAx	Input	Bank Address Inputs: BA0 - BA1 define to which bank an Active, Read, Write or Precharge command is being applied. Bank address also determines which mode register is to be accessed during a MRS cycle.
Ax	Input	Address Inputs: Provide the row address for ACTIVATE Commands and the column address for Read/Write commands to select one location out of the memory array in the respective bank. A10/AP, A12/BC_n, RAS_n/A16, CAS_n/A15 and WE_n/A14 have additional functions. See other rows. The address inputs also provide the op-code during Mode Register Set commands. A17 is only defined for 16 Gb x4 SDRAM configurations.
A10 / AP	Input	Auto-precharge: A10 is sampled during Read/Write commands to determine whether Autoprecharge should be performed to the accessed bank after the Read/Write operation. (HIGH: Autoprecharge; LOW: no Autoprecharge). A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by bank addresses.

Symbol	Type	Function
A12/BC_n	Input	Burst Chop: A12/BC_n is sampled during Read and Write commands to determine if burst chop (on-thefly) will be performed. (HIGH, no burst chop; LOW: burst chopped). See command truth table for details.
Parity	Input	Command and Address Parity Input: DDR4 Supports Even Parity check in SDRAMs with MR setting. Once it's enabled via Register in MR5, then SDRAM calculates Parity with ACT_n, RAS_n/A16, CAS_n/A15, WE_n/A14, BG0-BG1, BA0-BA1, A17-A0. Input parity should be maintained at the rising edge of the clock and at the same time with command & address with CS_n LOW
SAx	Input	Serial address inputs: Used to configure the temperature sensor/SPD EEPROM address range on the I2C bus.
SCL	Input	Serial clock for temperature sensor/SPD EEPROM: Used to synchronize communication to and from the temperature sensor/SPD EEPROM on the I2C bus.
RESET_n	CMOS Input	Active Low Asynchronous Reset: Reset is active when RESET_n is LOW, and inactive when RESET_n is HIGH. RESET_n must be HIGH during normal operation.
DQx, CBx	I/O	Data Input/ Output: Bi-directional data bus. If CRC is enabled via Mode register then CRC code is added at the end of Data Burst. Any DQ from DQ0-DQ3 may indicate the internal Vref level during test via Mode Register Setting MR4 A4=High. Refer to vendor specific data sheets to determine which DQ is used.
DQSx_t-DQSx_c	I/O	Data Strobe: output with read data, input with write data. Edge-aligned with read data, centered in write data. The data strobe DQS_t is paired with differential signals DQS_c, respectively, to provide differential pair signaling to the system during reads and writes. DDR4 SDRAM supports differential data strobe only and does not support single-ended.
DM_n/DBI_n/ TDQS_t (DMU_n, DBIU_n), (DML_n/ DBIL_n)	I/O	Input data mask and data bus inversion: DM_n is an input mask signal for write data. Input data is masked when DM_n is sampled LOW coincident with that input data during a write access. DM_n is sampled on both edges of DQS. DM is multiplexed with the DBI function by the mode register A10, A11, and A12 settings in MR5. For a x8 device, the function of DM or TDQS is enabled by the mode register A11 setting in MR1. DBI_n is an input/output identifying whether to store/output the true or inverted data. If DBI_n is LOW, the data will be stored/ output after inversion inside the DDR4 device and not inverted if DBI_n is HIGH. TDQS is only supported in x8 SDRAM configurations (TDQS is not valid for UDIMMs).
SDA	I/O	Serial Data: Bidirectional signal used to transfer data in or out of the EEPROM or EEPROM/TS combo device.
ALERT_n	Output	Alert: It has multi functions such as CRC error flag, Command and Address Parity error flag as Output signal. If there is error in CRC, then ALERT_n goes LOW for the period time interval and goes back HIGH. If there is error in Command Address Parity Check, then ALERT_n goes LOW for relatively long period until ongoing SDRAM internal recovery transaction is complete. During Connectivity Test mode this pin functions as an input.
EVENT_n	Output	Temperature event: The EVENT_n pin is asserted by the temperature sensor when critical temperature thresholds have been exceeded. This pin has no function (NF) on modules without temperature sensors.

Symbol	Type	Function
TDQS_t TDQS_c (x8 DRAM-based RDIMM only)	Output	Termination data strobe: When enabled via the mode register, the DRAM device enables the same RTT termination resistance on TDQS_t and TDQS_c that is applied to DQS_t and DQS_c. When the TDQS function is disabled via the mode register, the DM/TDQS_t pin provides the data mask (DM) function, and the TDQS_c pin is not used. The TDQS function must be disabled in the mode register for both the x4 and x16 configurations. The DM function is supported only in x8 and x16 configurations. DM, DBI, and TDQS are a shared pin and are enabled/disabled by mode register settings. For more information about TDQS, see the DDR4 DRAM component datasheet (TDQS_t and TDQS_c are not valid for UDIMMs).
VDD	Supply	Module power supply: 1.2V (TYP).
VPP	Supply	DRAM activating power supply: 2.5V –0.125V / +0.250V.
VREFCA	Supply	Reference voltage for control, command, and address pins.
VSS	Supply	Ground.
VTT	Supply	Power supply for termination of address, command, and control VDD/2.
VDDSPD	Supply	Power supply used to power the I2C bus for SPD.
RFU	-	Reserved for Future Use: No on DIMM electrical connection is present
NC	-	No Connect: No on DIMM electrical connection is present

3 General Description

3.1 General Description

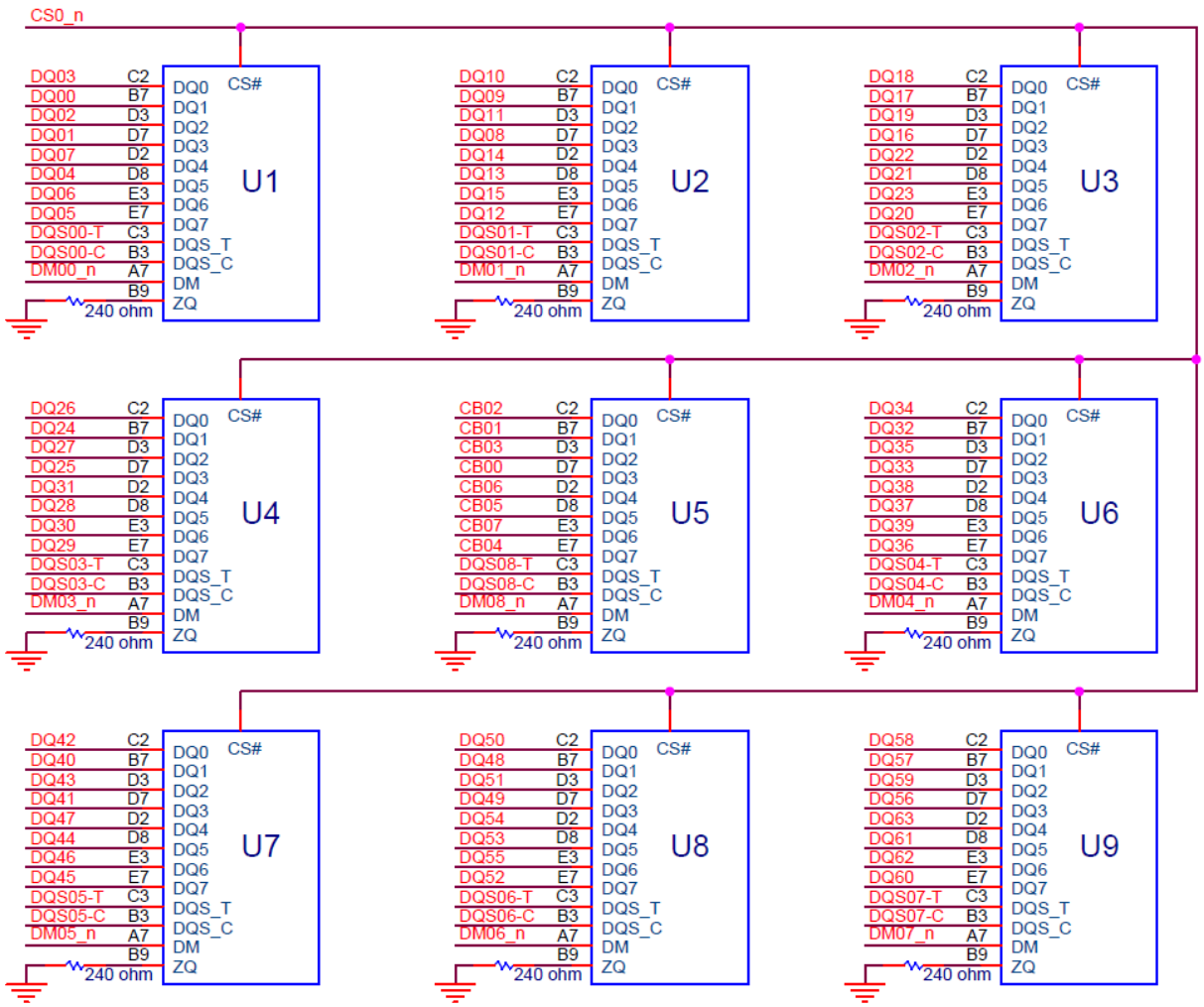
High-speed DDR4 SDRAM modules use DDR4 SDRAM devices with 2 or 4 internal memory bank groups. DDR4 SDRAM modules utilizing 4- and 8-bit-wide DDR4 SDRAM have 4 internal bank groups consisting of 4 memory banks each, providing a total of 16 banks. Sixteen-bit-wide DDR4 SDRAM has 2 internal bank groups consisting of 4 memory banks each, providing a total of 8 banks. DDR4 SDRAM modules benefit from DDR4 SDRAM's use of an 8n-prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single READ or WRITE operation for the DDR4 SDRAM effectively consists of a single 8n-bit-wide, four-clock data transfer at the internal DRAM core and eight corresponding n-bit wide, one-half-clock-cycle data transfers at the I/O pins.
DDR4 modules use two sets of differential signals: DQS, DQS# to capture data and CK and CK# to capture commands, addresses, and control signals. Differential clocks and data strobes ensure exceptional noise immunity for these signals and provide precise crossing points to capture input signals.

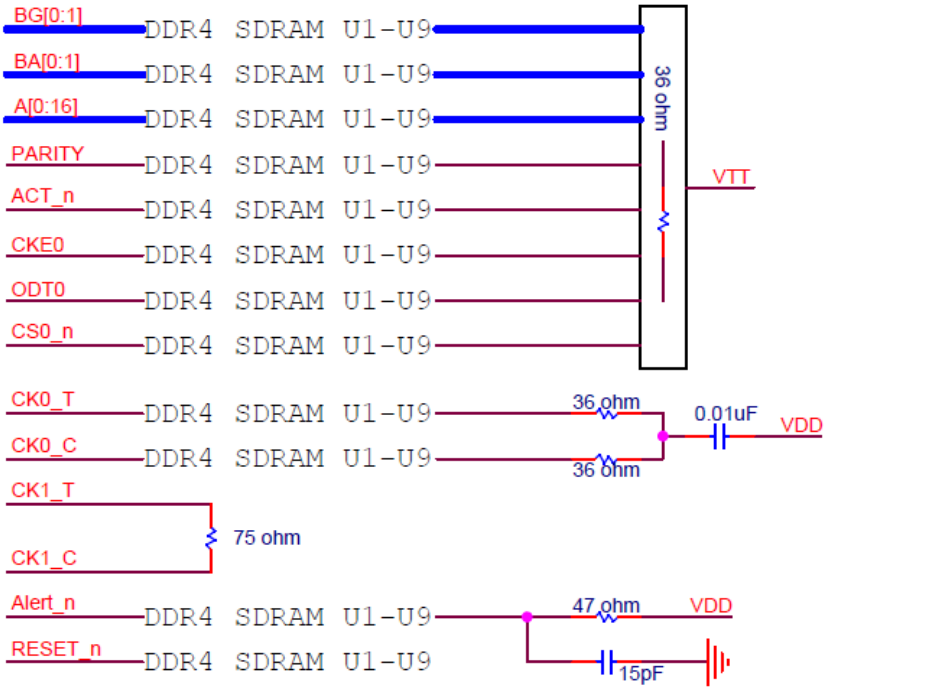
3.2 Serial Presence-Detect EEPROM Operation

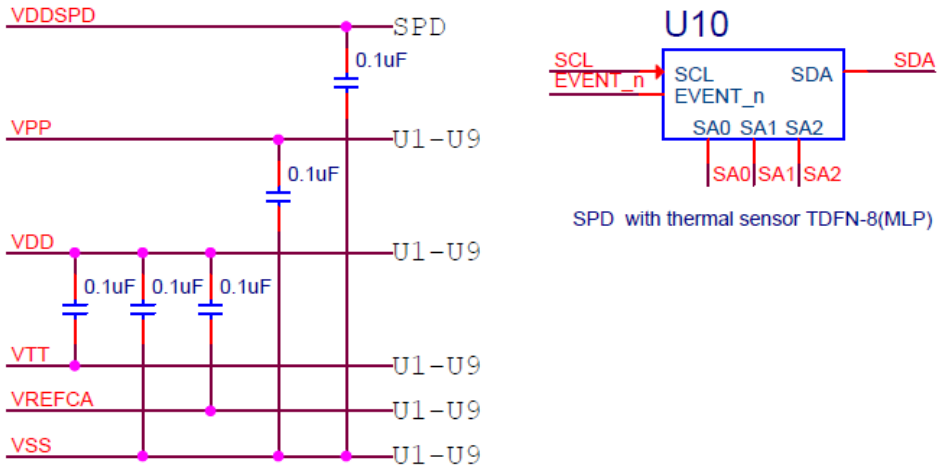
DDR4 SDRAM modules incorporate serial presence-detect. The SPD data is stored in a 512-byte EEPROM. System READ/WRITE operations between the master (system logic) and the slave EEPROM device occur via a standard I2C bus using the DIMM’s SCL (clock) SDA (data), and SA (address) pins. Write protect (WP) is connected to VSS, permanently disabling hardware write protection.

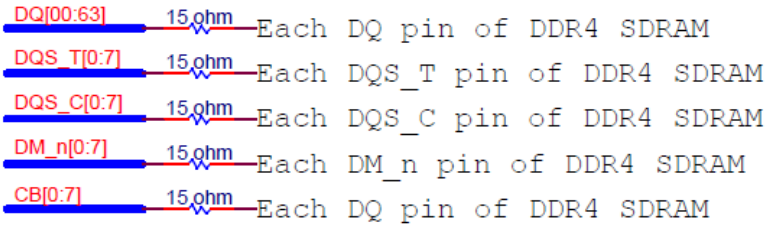
3.3 Function Block Diagram

Figure 1 – Function Block Diagram_SCC08GE03C2F1V-32AA




BG[0:1]
DDR4 SDRAM U1-U9
BA[0:1]
DDR4 SDRAM U1-U9
A[0:16]
DDR4 SDRAM U1-U9
PARITY
DDR4 SDRAM U1-U9
ACT_n
DDR4 SDRAM U1-U9
CKE0
DDR4 SDRAM U1-U9
ODT0
DDR4 SDRAM U1-U9
CS0_n
DDR4 SDRAM U1-U9
36 ohm
VTT
CK0_T
DDR4 SDRAM U1-U9
CK0_C
DDR4 SDRAM U1-U9
36 ohm
36 ohm
0.01uF
VDD
CK1_T
75 ohm
CK1_C
Alert_n
DDR4 SDRAM U1-U9
RESET_n
DDR4 SDRAM U1-U9
47 ohm
VDD
15pF


VDDSPD
SPD
0.1uF
VPP
U1-U9
0.1uF
VDD
U1-U9
0.1uF
0.1uF
0.1uF
VTT
U1-U9
VREFCA
U1-U9
VSS
U1-U9
U10
SCL
EVENT_n
SCL
EVENT_n
SDA
SDA
SA0 SA1 SA2
SA0
SA1
SA2
SPD with thermal sensor TDFN-8(MLP)


DQ[00:63]
15 ohm
Each DQ pin of DDR4 SDRAM
DQS_T[0:7]
15 ohm
Each DQS_T pin of DDR4 SDRAM
DQS_C[0:7]
15 ohm
Each DQS_C pin of DDR4 SDRAM
DM_n[0:7]
15 ohm
Each DM_n pin of DDR4 SDRAM
CB[0:7]
15 ohm
Each DQ pin of DDR4 SDRAM

3.4 DQ Map

Table 6 - DQ Map_SCC08GE03C2F1V-32AA

Module Pin No.	Module DQ	Damping RES.	IC NO.	IC DQ	Module Pin No.	Module DQ	Damping RES.	IC NO.	IC DQ
5	0	RN1(3-6)	U1	1	16	8	RN4(3-6)	U2	3
150	1	RN1(4-5)		3	161	9	RN4(4-5)		1
12	2	RN3(3-6)		2	23	10	RN6(3-6)		0
157	3	RN3(4-5)		0	168	11	RN6(4-5)		2
3	4	RN1(1-8)		5	14	12	RN4(1-8)		7
148	5	RN1(2-7)		7	159	13	RN4(2-7)		5
10	6	RN3(1-8)		6	21	14	RN6(1-8)		4
155	7	RN3(2-7)		4	166	15	RN6(2-7)		6
27	16	RN7(3-6)	U3	3	38	24	RN10(3-6)	U4	1
172	17	RN7(4-5)		1	183	25	RN10(4-5)		3
34	18	RN9(3-6)		0	45	26	RN12(3-6)		0
179	19	RN9(4-5)		2	190	27	RN12(4-5)		2
25	20	RN7(1-8)		7	36	28	RN10(1-8)		5
170	21	RN7(2-7)		5	181	29	RN10(2-7)		7
32	22	RN9(1-8)		4	43	30	RN12(1-8)		6
177	23	RN9(2-7)		6	188	31	RN12(2-7)		4
49	CB0	RN13(3-6)	U5	3	97	32	RN16(3-6)	U6	1
194	CB1	RN13(4-5)		1	242	33	RN16(4-5)		3
56	CB2	RN15(3-6)		0	104	34	RN18(3-6)		0
201	CB3	RN15(4-5)		2	249	35	RN18(4-5)		2
47	CB4	RN13(1-8)		7	95	36	RN16(1-8)		7
192	CB5	RN13(2-7)		5	240	37	RN16(2-7)		5
54	CB6	RN15(1-8)		4	102	38	RN18(1-8)		4
199	CB7	RN15(2-7)		6	247	39	RN18(2-7)		6
108	40	RN19(3-6)	U7	1	119	48	RN22(3-6)	U8	1
253	41	RN19(4-5)		3	264	49	RN22(4-5)		3
115	42	RN21(3-6)		0	126	50	RN24(3-6)		0
260	43	RN21(4-5)		2	271	51	RN24(4-5)		2
106	44	RN19(1-8)		5	117	52	RN22(1-8)		7
251	45	RN19(2-7)		7	262	53	RN22(2-7)		5
113	46	RN21(1-8)		6	124	54	RN24(1-8)		4
258	47	RN21(2-7)		4	269	55	RN24(2-7)		6
130	56	RN25(3-6)	U9	3					
275	57	RN25(4-5)		1					
137	58	RN27(3-6)		0					
282	59	RN27(4-5)		2					
128	60	RN25(1-8)		7					
273	61	RN25(2-7)		5					
135	62	RN27(1-8)		6					
280	63	RN27(2-7)		4					

4 Electrical Characteristics

This chapter contains speed grade definition, AC timing parameter and ODT tables.

4.1 Absolute Maximum Ratings

Attention: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table 7 - Absolute Maximum Ratings

Symbol	Parameter	Rating		Unit	Note
		Min.	Max.		
V_{DD}	Voltage on V_{DD} pin relative to V_{SS}	-0.4	+1.5	V	
V_{DDQ}	Voltage on V_{DDQ} pin relative to V_{SS}	-0.4	+1.5	V	
V_{PP}	Voltage on V_{PP} pin relative to V_{SS}	-0.4	3.0	V	
V_{IN}, V_{OUT}	Voltage on any pin relative to V_{SS}	-0.4	+1.5	V	
T_{STG}	Storage Temperature	-50	+100	°C	

Attention: Stresses above the max. values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to integrated circuit.

Table 8 - DRAM Component Operating Temperature Range

Symbol	Parameter	Rating		Unit	Note
		Min.	Max.		
T_{CASE}	Operating Temperature	0	95	°C	1)2)3)4)

1) Operating Temperature is the case surface temperature on the center / top side of the DRAM.
2) The operating temperature ranges are the temperatures where all DRAM specification will be supported. During operation, the DRAM case temperature must be maintained between 0 - 95 °C under all other specification parameters.
3) Above 85 °C the Auto-Refresh command interval has to be reduced to t_{REFI}= 3.9 µs
4) When operating this product in the 85 °C to 95 °C T_{CASE} temperature range, the High Temperature Self Refresh has to be enabled by setting EMR(2) bit A7 to "1".

4.2 Operating Conditions

Table 9 - Supply Voltage Levels and AC / DC Operating Conditions

Parameter	Symbol	Values			Unit	Note
		Min.	Typ.	Max.		
Device Supply Voltage	V_{DD}	1.14	1.2	1.26	V	1),2),3)
Output Supply Voltage	V_{DDQ}	1.14	1.2	1.26	V	1),2),3)
Peak-to-Peak Voltage	V_{PP}	2.375	2.5	2.75	V	3)
Input Reference Voltage	V_{REF}	0.49 × V_{DD}	0.5 × V_{DDQ}	0.51 × V_{DD}	V	
DC Input Logic High	$V_{IH.CA(DC65)}$	V_{REFCA} + 0.065	—	V_{DD}	V	
DC Input Logic Low	$V_{IL.CA\ (DC65)}$	Vss	—	V_{REFCA} – 0.065	V	
AC Input Logic High	$V_{IH.CA(AC90)}$	V_{REF} + 0.09	—		V	
AC Input Logic Low	$V_{IL.CA\ (AC90)}$		—	V_{REF} –0.09	V	

Notes:

1) Under all conditions VDDQ must be less than or equal to VDD.
2) VDDQ tracks with VDD. AC parameters are measured with VDD and VDDQ tied together.
3) DC bandwidth is limited to 20MHz.

4.3 Module and Component Speed Grades

DDR4 components may exceed the listed module speed grades; module may not be available in all listed speed grades

Table 10 - Module and Component Speed Grades

Module Speed Grade	Component Speed Grade
-32AA	3200-22-22-22

4.4 I_{DD}/I_{PP} Specifications and Conditions

List of tables defining I_{DD} / I_{PP} Specifications and Conditions.

Table 11 - I_{DD} /I_{PP} Measurement Conditions

Symbol	Description
IDD0 IPP0	Operating One Bank Active-Precharge Current (AL=0) CKE: High; External clock: On; tCK, nRC, nRAS, CL: Refer to Component Datasheet for detail pattern; BL: 8[1]; AL: 0; CS_n: High between ACT and PRE; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: Cycling with one bank active at a time: 0,0,1,1,2,2,... ; Output Buffer and RTT: Enabled in Mode Registers[2]; ODT Signal: stable at 0; Pattern Details: Refer to Component Datasheet for detail pattern
IDD1 IPP1	Operating One Bank Active-Read-Precharge Current (AL=0) CKE: High; External clock: On; tCK, nRC, nRAS, nRCD, CL: Refer to Component Datasheet for detail pattern; BL: 8[1]; AL: 0; CS_n: High between ACT, RD and PRE; Command, Address, Bank Group Address, Bank Address Inputs, Data IO: partially toggling; DM_n: stable at 1; Bank Activity: Cycling with one bank active at a time: 0,0,1,1,2,2,... ; Output Buffer and RTT: Enabled in Mode Registers[2]; ODT Signal: stable at 0; Pattern Details: Refer to Component Datasheet for detail pattern
IDD2N IPP2N	Precharge Standby Current (AL=0) CKE: High; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 8[1]; AL: 0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling ; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers[2]; ODT Signal: stable at 0; Pattern Details: Refer to Component Datasheet for detail pattern
IDD2NT	Precharge Standby ODT Current CKE: High; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 8[1]; AL: 0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling ; Data IO: VSSQ; DM_n: stable at 1; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers[2]; ODT Signal: toggling according ; Pattern Details: Refer to Component Datasheet for detail pattern
IDD2P IPP2P	Precharge Power-Down Current CKE: Low; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 8[1]; AL: 0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: stable at 0; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers[2]; ODT Signal: stable at 0
IDD2Q	Precharge Quiet Standby Current CKE: High; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 8[1]; AL: 0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: stable at 0; Data IO: VDDQ; DM_n: stable at 1;Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers[2]; ODT Signal: stable at 0

Symbol	Description
IDD3N IPP3N	Active Standby Current CKE: High; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 8[1]; AL: 0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling Data IO: VDDQ; DM_n: stable at 1;Bank Activity: all banks open; Output Buffer and RTT: Enabled in Mode Registers[2]; ODT Signal: stable at 0; Pattern Details:Refer to Component Datasheet for detail pattern
IDD3P IPP3P	Active Power-Down Current CKE: Low; External clock: On; tCK, CL: sRefer to Component Datasheet for detail pattern; BL: 8[1]; AL: 0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: stable at 0; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: all banks open; Output Buffer and RTT: Enabled in Mode Registers[2]; ODT Signal: stable at 0
IDD4R IPP4R	Operating Burst Read Current CKE: High; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 8[2]; AL: 0; CS_n: High between RD; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling ; Data IO: seamless read data burst with different data between one burst and the next one according ; DM_n: stable at 1; Bank Activity: all banks open, RD commands cycling through banks: 0,0,1,1,2,2,... ; Output Buffer and RTT: Enabled in Mode Registers[2]; ODT Signal: stable at 0; Pattern Details: Refer to Component Datasheet for detail pattern
IDD4W IPP4W	Operating Burst Write Current CKE: High; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 8[1]; AL: 0; CS_n: High between WR; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling ; Data IO: seamless write data burst with different data between one burst and the next one ; DM_n: stable at 1; Bank Activity: all banks open, WR commands cycling through banks: 0,0,1,1,2,2,...; Output Buffer and RTT: Enabled in Mode Registers[2]; ODT Signal: stable at HIGH; Pattern Details: Refer to Component Datasheet for detail pattern
IDD5B IPP5B	Burst Refresh Current (1X REF) CKE: High; External clock: On; tCK, CL, nRFC: Refer to Component Datasheet for detail pattern; BL: 8[1]; AL: 0; CS_n: High between REF; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling ; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: REF command every nRFC ; Output Buffer and RTT: Enabled in Mode Registers[2]; ODT Signal: stable at 0; Pattern Details: Refer to Component Datasheet for detail pattern
IDD5F2 IPP5F2	Burst Refresh Current (2X REF) tRFC=tRFC_x2,
IDD5F4 IPP5F4	Burst Refresh Current (4X REF) tRFC=tRFC_x4,
IDD6N IPP6N	Self Refresh Current: Normal Temperature Range Tcase: 0 - 85°C; Low Power Array Self Refresh (LP ASR) : Normal4; CKE: Low; External clock: Off; CK_t and CK_c#: LOW; CL: Refer to Component Datasheet for detail pattern; BL: 8[1]; AL: 0; CS_n#, Command, Address, Bank Group Address, Bank Address, Data IO: High; DM n: stable at 1; Bank Activity: Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: MIDLEVEL
IDD6E IPP6E	Self-Refresh Current: Extended Temperature Range) TCase: 0 - 95°C; Low Power Array Self Refresh (LP ASR) : Extended4; CKE: Low; External clock: Off; CK_t and CK_c: LOW; CL: Refer to Component Datasheet for detail pattern; BL: 8[1]; AL: 0; CS_n, Command, Address, Bank Group Address, Bank Address, Data IO: High; DM_n:stable at 1; Bank Activity: Extended Temperature Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: MID-LEVEL

Symbol	Description
IDD6R IPP6R	Self-Refresh Current: Reduced Temperature Range TCase: 0 - 45°C; Low Power Array Self Refresh (LP ASR) : Reduced[4]; CKE: Low; External clock: Off; CK_t and CK_c#: LOW; CL: Refer to Component Datasheet for detail pattern; BL: 8[1]; AL: 0; CS_n#, Command, Address, Bank Group Address, Bank Address, Data IO: High; DM_n:stable at 1; Bank Activity: Extended Temperature Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers[2]; ODT Signal: MID-LEVEL
IDD6A IPP6A	Auto Self-Refresh Current TCase: 0 - 95°C; Low Power Array Self Refresh (LP ASR) : Auto[4]; CKE: Low; External clock: Off; CK_t and CK_c#: LOW; CL: Refer to Component Datasheet for detail pattern; BL: 8[1]; AL: 0; CS_n#, Command, Address, Bank Group Address, Bank Address, Data IO: High; DM_n:stable at 1; Bank Activity: Auto Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers[2]; ODT Signal: MID-LEVEL
IDD7 IPP7	Operating Bank Interleave Read Current CKE: High; External clock: On; tCK, nRC, nRAS, nRCD, nRRD, nFAW, CL: Refer to Component Datasheet for detail pattern; BL: 8[1]; AL: CL-1; CS_n: High between ACT and RDA; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling ; Data IO: read data bursts with different data between one burst and the next one ; DM_n: stable at 1; Bank Activity: two times interleaved cycling through banks (0, 1, ...7) with different addressing; Output Buffer and RTT: Enabled in Mode Registers[2]; ODT Signal: stable at 0; Pattern Details: Refer to Component Datasheet for detail pattern
IDD8 IPP8	Maximum Power Down Current TBD

Notes :

1. Burst Length: BL8 fixed by MRS: set MR0 [A1:0=00].

2. Output Buffer Enable - set MR1 [A12 = 0] : Qoff = Output buffer enabled - set MR1 [A2:1 = 00] : Output Driver Impedance Control = RZQ/7 RTT_Nom enable - set MR1 [A10:8 = 011] : RTT_NOM = RZQ/6 RTT_WR enable - set MR2 [A10:9 = 01] : RTT_WR = RZQ/2 RTT_PARK disable - set MR5 [A8:6 = 000]

3. CAL enabled : set MR4 [A8:6 = 001] : 1600MT/s 010] : 1866MT/s, 2133MT/s 011] : 2400MT/s Gear Down mode enabled :set MR3 [A3 = 1] : 1/4 Rate DLL disabled : set MR1 [A0 = 0] CA parity enabled :set MR5 [A2:0 = 001] : 1600MT/s,1866MT/s, 2133MT/s 010] : 2400MT/s Read DBI enabled : set MR5 [A12 = 1] Write DBI enabled : set :MR5 [A11 = 1]

4. Low Power Array Self Refresh (LP ASR) : set MR2 [A7:6 = 00] : Normal 01] : Reduced Temperature range 10] : Extended Temperature range 11] : Auto Self Refresh

Table 12 – I_{DD} Specification for SCC08GE03C2F1V-32AA

Product Type	SCC08GE03C2F1V-32AA	Unit	Note
Organization	8GB		
	1 Rank (×8)		
	×72		
	-32AA		
Symbol	Current		
IDD0	969.3	mA	2)
IDD1	1161	mA	2)
IDD2N	741.6	mA	3)
IDD2NT	834.3	mA	2)
IDD2P	498.6	mA	3)
IDD2Q	681.3	mA	3)
IDD3N	792.9	mA	3)
IDD3P	520.2	mA	3)
IDD4R	1762	mA	2)
IDD4W	1876	mA	2)
IDD5B	3190	mA	2)
IDD5F2	2456	mA	2)
IDD5F4	2631	mA	2)
IDD6N	444.6	mA	3)
IDD6E	560.7	mA	3)
IDD6R	357.3	mA	3)
IDD6A	560.7	mA	3)
IDD7	2763	mA	2)
IDD8	344.7	mA	3)

Notes:

1) Calculated values from Device data.
2) One module rank in the active IDD/IPP, the other rank in IDD2P/IPP3N.
3) All ranks in this IDD/IPP condition

Table 13 – I_{PP} Specification for SCC08GE03C2F1V-32AA

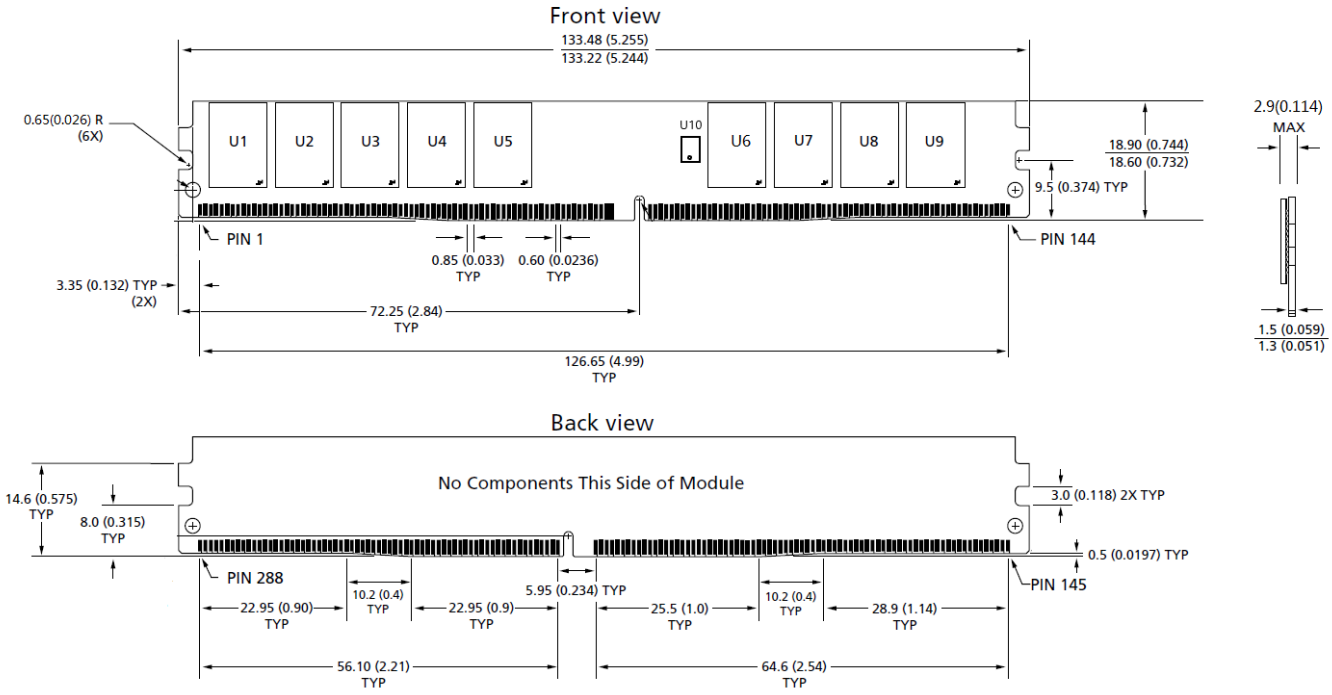
Product Type	SCC08GE03C2F1V-32AA	Unit	Note
Organization	8GB		
	1Rank (×8)		
	×72		
	-32AA		
Symbol	Current		
IPP0	88.2	mA	2)
IPP1	88.2	mA	2)
IPP2N	37.8	mA	3)
IPP2P	37.8	mA	3)
IPP3N	37.8	mA	3)
IPP3P	37.8	mA	3)
IPP4R	38.7	mA	2)
IPP4W	38.7	mA	2)
IPP5B	405	mA	2)
IPP6N	58.5	mA	3)
IPP6E	80.1	mA	3)
IPP6R	43.2	mA	3)
IPP6A	80.1	mA	3)
IPP7	298.8	mA	2)
IPP8	37.8	mA	3)

Notes:

1) Calculated values from Device data.
2) One module rank in the active IDD/IPP, the other rank in IDD2P/IPP3N.
3) All ranks in this IDD/IPP condition

5 Package Dimensions

Figure 2 – Package Dimensions_SCC08GE03C2F1V-32AA



Notes:
1. All dimensions are in millimeters (inches); MAX/MIN or typical (TYP) where noted.
2. The dimensional diagram is for reference only.

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