Jun. 2021

SCB13H1G160DF

1Gbit DDR3 SDRAM
EU RoHS Compliant Products

Data Sheet

Rev. A

Revision History		
Date	**Revision**	**Subjects (major changes since last revision)**
2021-06-28	A	Initial Release

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Contents

1 Features

The 1Gbit DDR3 SDRAM offers the following key features:

- JEDEC Standard Compliant
- Power supplies: V_{DD} & V_{DDQ} = +1.35V (1.283V ~ 1.45V)
- Backward compatible to V_{DD} & V_{DDQ} = +1.5V ±0.075V
- Operating temperature range: (Commercial)
  - Normal operating temperature: T_C = 0~85°C
  - Extended temperature: T_C = 85~95°C
- Supports JEDEC clock jitter specification
- Fully synchronous operation
- Fast clock rate: 667/800/933MHz
- Differential Clock, CK & CK#
- Bidirectional differential data strobe
  - DQS & DQS#
- 8 internal banks for concurrent operation
- 8n-bit prefetch architecture
- Pipelined internal architecture
- Precharge & active power down
- Programmable Mode & Extended Mode registers
- Additive Latency (AL): 0, CL-1, CL-2
- Programmable Burst lengths: 4, 8
- Burst type: Sequential / Interleave
- Output Driver Impedance Control
- Auto Refresh and Self Refresh
- Average refresh period
  - 8192 cycles/64ms (7.8us at 0°C ≦ T_C ≦ +85°C)
  - 8192 cycles/32ms (3.9us at +85°C ≦ T_C ≦ +95°C)
- Write Leveling
- ZQ Calibration
- Dynamic ODT (Rtt_Nom & Rtt_WR)
- RoHS compliant
- 96-ball 7.5 x 13 x 1.0mm FBGA package
  - Pb and Halogen Free

2 Product List

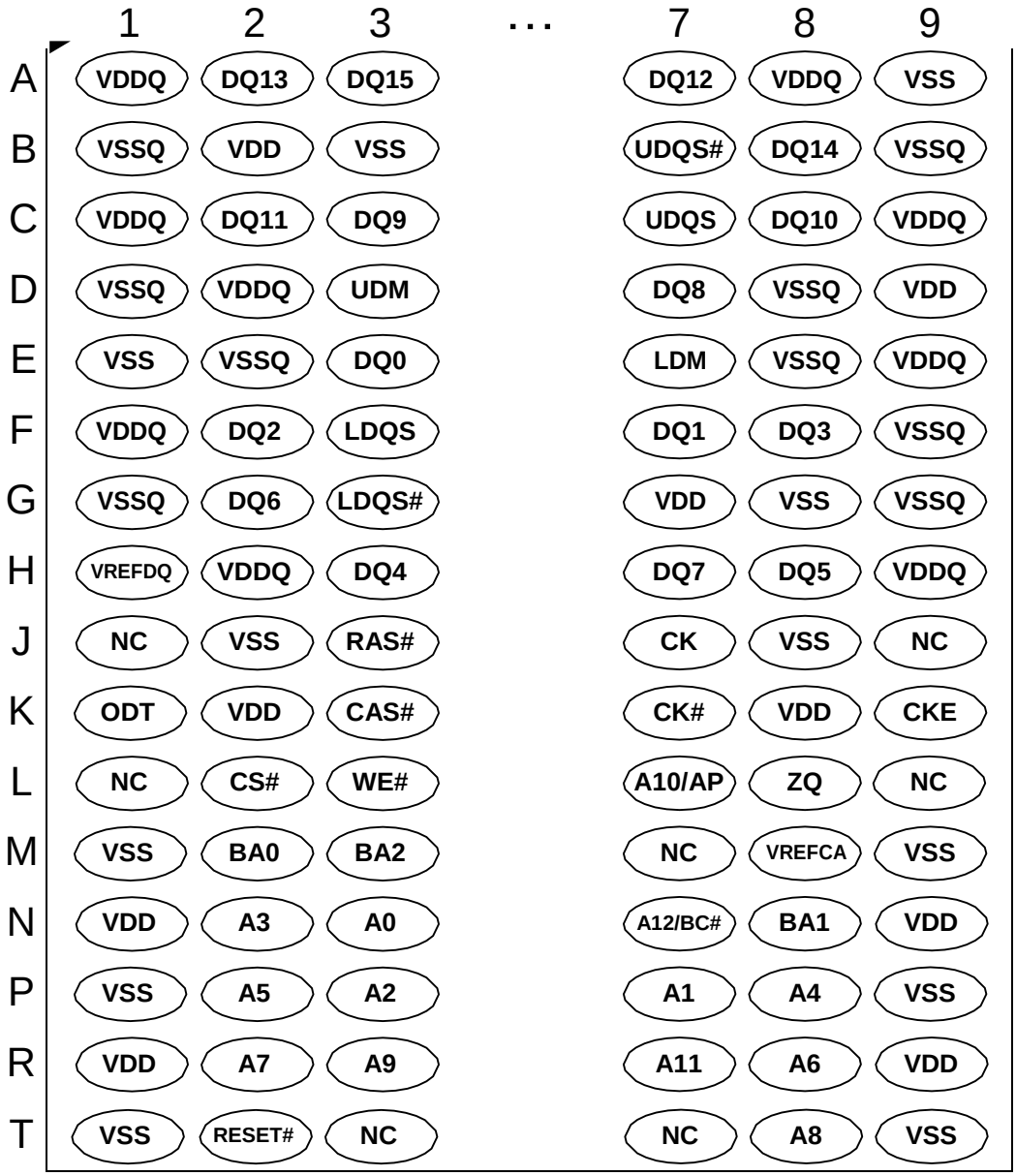
Table 1 shows all possible products within the 1Gbit DDR3 SDRAM component generation.

Table 1 - Ordering Information for 1Gbit DDR3 Component

UniIC Part Number	Max. Clock frequency	CAS-RCD-RP latencies	Speed Sort Name	Package
1Gbit DDR3 SDRAM Components				
Commercial Temperature Range (0 °C~ +95 °C)				
SCB13H1G160DF-11M	933 MHz	13-13-13	DDR3–1866M	PG-FBGA-96

3 Ball Configuration

Figure 1 - Ball out for 64 Mb ×16 Components (FBGA-96)



4 Ball Description

Table 2 - Input / Output Signal Functional Description

Symbol	Type	Description
CK, CK#	Input	**Differential Clock:** CK and CK# are driven by the system clock. All SDRAM input signals are sampled on the crossing of positive edge of CK and negative edge of CK#. Output (Read) data is referenced to the crossings of CK and CK# (both directions of crossing).
CKE	Input	**Clock Enable:** CKE activates (HIGH) and deactivates (LOW) the CK signal. If CKE goes LOW synchronously with clock, the internal clock is suspended from the next clock cycle and the state of output and burst address is frozen as long as the CKE remains LOW. When all banks are in the idle state, deactivating the clock controls the entry to the Power Down and Self Refresh modes.
BA0-BA2	Input	**Bank Address:** BA0-BA2 define to which bank the BankActivate, Read, Write, or Bank Precharge command is being applied.
A0-A12	Input	**Address Inputs:** A0-A12 is sampled during row address (A0-A12) for Active commands and the column address (A0-A9) for Read/Write commands to select one location out of the memory array in the respective bank. (A10/AP and A12/BC# have additional functions). The address inputs also provide the op-code during Mode Register Set commands.
A10/AP	Input	**Auto-Precharge:** A10 is sampled during Read/Write commands to determine whether Autoprecharge should be performed to the accessed bank after the Read/Write operation. (HIGH: Autoprecharge; LOW: no Autoprecharge). A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH).
A12/BC#	Input	**Burst Chop:** A12/BC# is sampled during Read and Write commands to determine if burst chop (on the fly) will be performed. (HIGH - no burst chop; LOW - burst chopped).
CS#	Input	**Chip Select:** CS# enables (sampled LOW) and disables (sampled HIGH) the command decoder. All commands are masked when CS# is sampled HIGH. It is considered part of the command code.
RAS#	Input	**Row Address Strobe:** The RAS# signal defines the operation commands in conjunction with the CAS# and WE# signals and is latched at the crossing of positive edges of CK and negative edge of CK#. When RAS# and CS# are asserted "LOW" and CAS# is asserted "HIGH" either the BankActivate command or the Precharge command is selected by the WE# signal. When the WE# is asserted "HIGH" the BankActivate command is selected and the bank designated by BA is turned on to the active state. When the WE# is asserted "LOW" the Precharge command is selected and the bank designated by BA is switched to the idle state after the precharge operation.
CAS#	Input	**Column Address Strobe:** The CAS# signal defines the operation commands in conjunction with the RAS# and WE# signals and is latched at the crossing of positive edges of CK and negative edge of CK#. When RAS# is held "HIGH" and CS# is asserted "LOW" the column access is started by asserting CAS# "LOW". Then, the Read or Write command is selected by asserting WE# “HIGH" or “LOW".
WE#	Input	**Write Enable:** The WE# signal defines the operation commands in conjunction with the RAS# and CAS# signals and is latched at the crossing of positive edges of CK and negative edge of CK#. The WE# input is used to select the BankActivate or Precharge command and Read or Write command.

Symbol	Type	Description
LDQS, LDQS# UDQS UDQS#	Input / Output	**Bidirectional Data Strobe:** Specifies timing for Input and Output data. Read Data Strobe is edge triggered. Write Data Strobe provides a setup and hold time for data and DQM. LDQS is for DQ0~7, UDQS is for DQ8~15. The data strobes LDOS and UDQS are paired with LDQS# and UDQS# to provide differential pair signaling to the system during both reads and writes.
LDM, UDM	Input	**Data Input Mask:** Input data is masked when DM is sampled HIGH during a write cycle. LDM masks DQ0-DQ7, UDM masks DQ8-DQ15.
DQ0-DQ15	Input / Output	**Data I/O:** The DQ0-DQ15 input and output data are synchronized with positive and negative edges of DQS and DQS#. The I/Os are byte-maskable during Writes.
ODT	Input	**On Die Termination:** ODT (registered HIGH) enables termination resistance internal to the DDR3L SDRAM. When enabled, ODT is applied to each DQ, DQS, DQS#. The ODT pin will be ignored if Mode-registers, MR1and MR2, are programmed to disable RTT.
RESET#	Input	**Active Low Asynchronous Reset:** Reset is active when RESET# is LOW, and inactive when RESET# is HIGH. RESET# must be HIGH during normal operation. RESET# is a CMOS rail to rail signal with DC high and low at 80% and 20% of VDD.
V_{DD}	Supply	**Power Supply:** +1.35V -0.067V/+0.1V.
V_{SS}	Supply	**Ground**
V_{DDQ}	Supply	**DQ Power:** +1.35V -0.067V/+0.1V.
V_{SSQ}	Supply	**DQ Ground**
V_{REFCA}	Supply	**Reference voltage for CA**
V_{REFDQ}	Supply	**Reference voltage for DQ**
ZQ	Supply	**Reference pin for ZQ calibration.**
NC	-	**No Connect:** These pins should be left unconnected.

5 Electrical Specifications

Table 3 - IDD Specification parameters and test conditions (V_{DD} = 1.35V, T_{OPER} = 0~85 °C)

Parameter & Test Condition	Symbol	1866	Unit
		Max	
Operating One Bank Active-Precharge Current **CKE:** High; **External clock:** On; **BL:** 8[*1]; **AL:** 0; **CS#**: High between ACT and PRE; **Command, Address, Bank Address Inputs:** partially toggling; **Data IO:** MID-LEVEL; **DM**:stable at 0; **Bank Activity:** Cycling with one bank active at a time: 0,0,1,1,2,2,...;**Output Buffer and RTT:** Enabled in Mode Registers[*2]; **ODT Signal:** stable at 0.	I_{DD0}	68	mA
Operating One Bank Active-Read-Precharge Current **CKE:** High; **External clock:** On; **BL:** 8[*1, 5]; **AL:**0; **CS#**: High between ACT, RDand PRE; **Command, Address, Bank Address Inputs, Data IO:** partially toggling; **DM**:stable at 0; **Bank Activity:** Cycling with one bank active at a time: 0,0,1,1,2,2,...; **Output Buffer and RTT:** Enabled in Mode Registers[*2]; **ODT Signal:** stable at 0.	I_{DD1}	88	mA
Precharge Standby Current **CKE**: High; **External clock:** On; **BL:** 8[*1]; **AL:** 0; **CS#**: stable at 1; **Command, Address, Bank Address Inputs:** partially toggling; **Data IO:** MID-LEVEL; **DM**:stable at 0; **Bank Activity:** all banks closed; **Output Buffer and RTT:** Enabled in Mode Registers[*2]; **ODT Signal:** stable at 0.	I_{DD2N}	45	mA
Precharge Power-Down Current Slow Exit **CKE:** Low; **External clock:** On; **BL:** 8[*1]; **AL:** 0; **CS#**: stable at 1; **Command, Address, Bank Address Inputs:** stable at 0; **Data IO:** MID-LEVEL; **DM**:stable at 0; **Bank Activity:** all banks closed; **Output Buffer and RTT:** Enabled in Mode Registers[*2]; **ODT Signal:** stable at 0; **Precharge Power Down Mode**: Slow Exit.[*3]	I_{DD2P0}	15	mA
Precharge Power-Down Current Fast Exit **CKE:** Low; **External clock:** On; **BL:** 8[*1]; **AL:** 0; **CS#**: stable at 1; **Command, Address, Bank Address Inputs:** stable at 0; **Data IO:** MID-LEVEL; **DM**:stable at 0; **Bank Activity:** all banks closed; **Output Buffer and RTT:** Enabled in Mode Registers[*2]; **ODT Signal:** stable at 0; **Precharge Power Down Mode**: Fast Exit.[*3]	I_{DD2P1}	25	mA
Precharge Quiet Standby Current **CKE**: High; **External clock:** On; **BL:** 8[*1]; **AL:** 0; **CS#**: stable at 1; **Command, Address, Bank Address Inputs:** stable at 0; **Data IO:** MID-LEVEL; **DM**:stable at 0;**Bank Activity:** all banks closed; **Output Buffer and RTT:** Enabled in Mode Registers[*2]; **ODT Signal:** stable at 0.	I_{DD2Q}	40	mA
Active Standby Current **CKE**: High; **External clock:** On; **BL:** 8[*1]; **AL:** 0; **CS#**: stable at 1; **Command, Address, Bank Address Inputs:** partially toggling; **Data IO:** MID-LEVEL; **DM**:stable at 0;**Bank Activity:** all banks open; **Output Buffer and RTT:** Enabled in Mode Registers[*2]; **ODT Signal:** stable at 0.	I_{DD3N}	53	mA
Active Power-Down Current **CKE:** Low; **External clock:** On; **BL:** 8[*1]; **AL:** 0; **CS#**: stable at 1; **Command, Address, Bank Address Inputs:** stable at 0; **Data IO:** MID-LEVEL; **DM**:stable at 0; **Bank Activity:** all banks open; **Output Buffer and RTT:** Enabled in Mode Registers[*2]; **ODT Signal:** stable at 0	I_{DD3P}	28	mA
Operating Burst Read Current **CKE:** High; **External clock:** On; **BL:** 8[*1, 5]; **AL:** 0; **CS#**: High between RD; **Command, Address, Bank Address Inputs:** partially toggling; **DM**:stable at 0; **Bank Activity:** all banks open, RD commands cycling through banks: 0,0,1,1,2,2,...; **output Buffer and RTT:** Enabled in Mode Registers[*2]; **ODT Signal:** stable at 0.	I_{DD4R}	155	mA

Parameter & Test Condition		Symbol	1866	Unit
			Max	
Operating Burst Write Current **CKE:** High; **External clock:** On; **BL:** 8[*1]; **AL:** 0; **CS#**: High between WR; **Command, Address, Bank Address Inputs:** partially toggling; **DM:** stable at 0; **Bank Activity:** all banks open. **Output Buffer and RTT:** Enabled in Mode Registers[*2]; **ODT Signal:** stable at HIGH.		I_{DD4W}	170	mA
Burst Refresh Current **CKE:** High; **External clock:** On; **BL:** 8[*1]; **AL:** 0; **CS#**: High between tREF; **Command, Address, Bank Address Inputs:** partially toggling; **Data IO:** MID- LEVEL; **DM**:stable at 0; **Bank Activity:** REF command every tRFC; **Output Buffer and RTT:** Enabled in Mode Registers[*2]; **ODT Signal:** stable at 0.		I_{DD5B}	100	mA
Self Refresh Current: **Self-Refresh Temperature Range (SRT):** Normal[4]; **CKE:** Low; **External clock:** Off; CK and CK#: LOW; **BL:** 8[*1]; **AL:** 0; **CS#, Command, Address, Bank Address, Data IO:** MID-LEVEL; **DM**:stable at 0; **Bank Activity:** Self-Refresh operation; **Output Buffer and RTT:** Enabled in Mode Registers[*2]; **ODT Signal:** MID-LEVEL	T_{CASE}: 0 - 85°C	I_{DD6}	15	mA
	T_{CASE}: 0 - 95°C	I_{DD6ET}	20	mA
Operating Bank Interleave Read Current **CKE:** High; **External clock:** On; **BL:** 8[*1, 5]; **AL:** CL-1; **CS#**: High between ACT and RDA; **Command, Address, Bank Address Inputs:** partially toggling; **DM**:stable at 0; **Output Buffer and RTT:** Enabled in Mode Registers[*2]; **ODT Signal:** stable at 0.		I_{DD7}	256	mA
RESET Low Current **RESET:** LOW; **External clock:** Off; **CK and CK#:** LOW; **CKE:** FLOATING; **CS#**, **Command, Address, Bank Address, Data IO:** FLOATING; **ODT Signal:** FLOATING RESET Low current reading is valid once power is stable and RESET has been LOW for at least 1ms.		I_{DD8}	10	mA

Note 1. Burst Length: BL8 fixed by MRS: set MR0 A[1,0]=00B.
Note 2. Output Buffer Enable: set MR1 A[12] = 0B; set MR1 A[5,1] = 01B; RTT_Nom enable: set MR1 A[9,6,2] = 011B; RTT_Wr enable: set MR2 A[10,9] = 10B.
Note 3. Precharge Power Down Mode: set MR0 A12=0B for Slow Exit or MR0 A12=1B for Fast Exit.
Note 4. Self-Refresh Temperature Range (SRT): set MR2 A7=0B for normal or 1B for extended temperature range.
Note 5. Read Burst Type: Nibble Sequential, set MR0 A[3] = 0B.
Note 6. Supporting 0 - 85 °C with full JEDEC AC & DC specifications. This is the minimum requirements for all operating temperature options. However, for applications operating in Extended Temperature 85°C ~ 95°C, some optional spec are required.

6 Electrical Characteristics and Recommended A.C. Operating Conditions

Table 4 - Electrical Characteristics and Recommended A.C. Operating Conditions (V_{DD}=1.35V, T_{OPER}=0~85°C)

Symbol	Parameter		1866		Unit	Note
			Min.	Max.		
t_{AA}	Internal read command to first data		13.91	20	ns	
t_{RCD}	ACT to internal read or write delay time		13.91	-	ns	
t_{RP}	PRE command period		13.91	-	ns	
t_{RC}	ACT to ACT or REF command period		47.91	-	ns	
t_{RAS}	ACTIVE to PRECHARGE command period		34	9 x t_{REFI}	ns	
$t_{CK(avg)}$	Average clock period	CL=5, CWL=5	-	-	ns	33
		CL=6, CWL=5	2.5	3.3	ns	33
		CL=7, CWL=6	1.875	<2.5	ns	33
		CL=8, CWL=6	1.875	<2.5	ns	33
		CL=9, CWL=7	1.5	<1.875	ns	33
		CL=10, CWL=7	1.5	<1.875	ns	33
		CL=11, CWL=8	1.25	<1.5	ns	33
		CL=12, CWL=8	1.25	<1.5	ns	33
		CL=13, CWL=9	1.07	<1.25	ns	33
$t_{CK\ (DLL\_OFF)}$	Minimum Clock Cycle Time (DLL off mode)		8	-	ns	6
$t_{CH(avg)}$	Average clock HIGH pulse width		0.47	0.53	t_{CK}	
$t_{CL(avg)}$	Average Clock LOW pulse width		0.47	0.53	t_{CK}	
t_{DQSQ}	DQS, DQS# to DQ skew, per group, per access		-	85	ps	13
t_{QH}	DQ output hold time from DQS, DQS#		0.38	-	t_{CK}	13
$t_{LZ(DQ)}$	DQ low-impedance time from CK, CK#		-390	195	ps	13,14
$t_{HZ(DQ)}$	DQ high impedance time from CK, CK#		-	195	ps	13,14
$t_{DS(base)}$	Data setup time to DQS, DQS# referenced to Vih(ac) / Vil(ac) levels	AC135	-	-	ps	17
		AC130	70	-	ps	17
$t_{DH(base)}$	Data hold time from DQS, DQS# referenced to Vih(dc) / Vil(dc) levels	DC90	75	-	ps	17
t_{DIPW}	DQ and DM Input pulse width for each input		320	-	ps	
t_{RPRE}	DQS,DQS# differential READ Preamble		0.9	-	t_{CK}	13,19
t_{RPST}	DQS, DQS# differential READ Postamble		0.3	-	t_{CK}	11,13
t_{QSH}	DQS, DQS# differential output high time		0.4	-	t_{CK}	13
t_{QSL}	DQS, DQS# differential output low time		0.4	-	t_{CK}	13
t_{WPRE}	DQS, DQS# differential WRITE Preamble		0.9	-	t_{CK}	1
t_{WPST}	DQS, DQS# differential WRITE Postamble		0.3	-	t_{CK}	1
t_{DQSCK}	DQS, DQS# rising edge output access time from rising CK, CK#		-195	195	ps	13
$t_{LZ(DQS)}$	DQS and DQS# low-impedance time (Referenced from RL - 1)		-390	195	ps	13, 14
$t_{HZ(DQS)}$	DQS and DQS# high-impedance time (Referenced from RL + BL/2)		-	195	ps	13, 14
t_{DQSL}	DQS, DQS# differential input low pulse width		0.45	0.55	t_{CK}	29, 31
t_{DQSH}	DQS, DQS# differential input high pulse width		0.45	0.55	t_{CK}	30, 31

Symbol	Parameter		1866		Unit	Note
			Min.	Max.		
t_{DQSS}	DQS, DQS# rising edge to CK, CK# rising edge		-0.27	0.27	t_{CK}	
t_{DSS}	DQS, DQS# falling edge setup time to CK, CK# rising edge		0.18	-	t_{CK}	32
t_{DSH}	DQS, DQS# falling edge hold time from CK, CK# rising edge		0.18	-	t_{CK}	32
t_{DLLK}	DLL locking time		512	-	t_{CK}	
t_{RTP}	Internal READ Command to PRECHARGE Command delay		max (4tCK, 7.5ns)	-	tCK	
t_{WTR}	Delay from start of internal write transaction to internal read command		max (4tCK, 7.5ns)	-	tCK	18
t_{WR}	WRITE recovery time		15	-	ns	18
t_{MRD}	Mode Register Set command cycle time		4	-	tCK	
t_{MOD}	Mode Register Set command update delay		max (12tCK, 15ns)	-	tCK	
t_{CCD}	CAS# to CAS# command delay		4	-	tCK	
$t_{DAL(min)}$	Auto precharge write recovery + prechargetime		WR + t_{RP}		t_{CK}	
t_{MPRR}	Multi-Purpose Register Recovery Time		1	-	t_{CK}	22
t_{RRD}	ACTIVE to ACTIVE command period		max ($4t_{CK}$, 6ns)	-	t_{CK}	
t_{FAW}	Four activate window		35	-	ns	
$t_{IS(base)}$	Command and Address setup time to CK, CK# referenced to Vih(ac) / Vil(ac) levels	AC160	-	-	ps	16
		AC135	65		ps	16,27
		AC125	150	-	ps	16,27
$t_{IH(base)}$	Command and Address hold time from CK, CK# referenced to Vih(dc) / Vil(dc) levels	DC90	110	-	ps	16
t_{IPW}	Control and Address Input pulse width for each input		535	-	ps	28
t_{ZQinit}	Power-up and RESET calibration time		512	-	t_{CK}	
t_{ZQoper}	Normal operation Full calibration time		256	-	t_{CK}	
t_{ZQCS}	Normal operation Short calibration time		64	-	t_{CK}	23
t_{XPR}	Exit Reset from CKE HIGH to a valid command		max ($5t_{CK}$, $t_{RFC(min)}$ + 10ns)	-	t_{CK}	
t_{XS}	Exit Self Refresh to commands not requiring a locked DLL		max ($5t_{CK}$, $t_{RFC(min)}$ + 10ns)	-	t_{CK}	
t_{XSDLL}	Exit Self Refresh to commands requiring a locked DLL		$t_{DLLK(min)}$	-	t_{CK}	
t_{CKESR}	Minimum CKE low width for Self Refresh entry to exit timing		$t_{CKE(min)}$ + $1t_{CK}$	-	t_{CK}	
t_{CKSRE}	Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down Entry (PDE)		max ($5t_{CK}$, 10 ns)	-	t_{CK}	
t_{CKSRX}	Valid Clock Requirement before Self Refresh Exit (SRX) or Power-Down Exit (PDX) or Reset Exit		max ($5t_{CK}$, 10 ns)	-	t_{CK}	
t_{XP}	Exit Power Down with DLL on to any valid command; Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL		max ($3t_{CK}$, 6 ns)	-	t_{CK}	
t_{XPDLL}	Exit Precharge Power Down with DLL frozen to commands requiring a lockedDLL		max ($10t_{CK}$, 24 ns)	-	t_{CK}	2

Symbol	Parameter		1866		Unit	Note
			Min.	Max.		
t_{CKE}	CKE minimum pulse width		max ($3t_{CK}$, 5 ns)	-	t_{CK}	
t_{CPDED}	Command pass disable delay		2	-	t_{CK}	
t_{PD}	Power Down Entry to Exit Timing		$t_{CKE\ (min)}$	9 x t_{REFI}		15
$t_{ACTPDEN}$	Timing of ACT command to Power Down entry		1	-	t_{CK}	20
t_{PRPDEN}	Timing of PRE or PREA command to Power Down entry		1	-	t_{CK}	20
t_{RDPDEN}	Timing of RD/RDA command to Power Down entry		RL+4+1	-	t_{CK}	
t_{WRPDEN}	Timing of WR command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)		WL+4+ (tWR/tCK)	-	tCK	9
$t_{WRAPDEN}$	Timing of WRA command to Power Down entry (BL8OTF, BL8MRS,BC4OTF)		WL+4+ WR+1	-	tCK	10
t_{WRPDEN}	Timing of WR command to Power Down entry (BC4MRS)		WL+2+ (tWR/tCK)	-	tCK	9
$t_{WRAPDEN}$	Timing of WRA command to Power Down entry (BC4MRS)		WL+2+ WR+1	-	tCK	10
$t_{REFPDEN}$	Timing of REF command to Power Down entry		1	-	tCK	20, 21
$t_{MRSPDEN}$	Timing of MRS command to Power Down entry		tMOD(min)	-		
ODTLon	ODT turn on Latency		WL - 2 = CWL + AL - 2		t_{CK}	
ODTLoff	ODT turn off Latency		WL - 2 = CWL + AL - 2			
ODTH4	ODT high time without write command or with write command and BC4		4	-	t_{CK}	
ODTH8	ODT high time with Write command and BL8		6	-	t_{CK}	
t_{AONPD}	Asynchronous RTT turn-on delay (Power- Down with DLL frozen)		2	8.5	ns	
t_{AOFPD}	Asynchronous RTT turn-off delay (Power-Down with DLL frozen)		2	8.5	ns	
t_{AON}	RTT turn-on		-195	195	ps	7
t_{AOF}	RTT_Nom and RTT_WR turn-off time from ODTLoff reference		0.3	0.7	t_{CK}	8
t_{ADC}	RTT dynamic change skew		0.3	0.7	t_{CK}	
t_{WLMRD}	First DQS/DQS# rising edge after write leveling mode is programmed		40	-	t_{CK}	3
$t_{WLDQSEN}$	DQS/DQS# delay after write leveling mode is programmed		25	-	t_{CK}	3
t_{WLS}	Write leveling setup time from rising CK, CK# crossing to rising DQS, DQS# crossing		140	-	ps	
t_{WLH}	Write leveling hold time from rising DQS, DQS# crossing to rising CK, CK# crossing		140	-	ps	
t_{WLO}	Write leveling output delay		0	7.5	ns	
t_{WLOE}	Write leveling output error		0	2	ns	
t_{RFC}	REF command to ACT or REF command time		110	-	ns	
t_{REFI}	Average periodic refresh interval	0°C to 85°C	-	7.8	µs	
		85°C to 95°C	-	3.9	µs	

Note 1. Actual value dependant upon measurement level.
Note 2. Commands requiring a locked DLL are: READ (and RAP) and synchronous ODT commands.
Note 3. The max values are system dependent.
Note 4. WR as programmed in mode register.
Note 5. Value must be rounded-up to next higher integer value.
Note 6. There is no maximum cycle time limit besides the need to satisfy the refresh interval, tREFI.

Note 7. For definition of RTT turn-on time tAON See “Timing Parameters”.
Note 8. For definition of RTT turn-off time tAOF See “Timing Parameters”.
Note 9. tWR is defined in ns, for calculation of tWRPDEN it is necessary to round up tWR / tCK to the next integer.
Note 10. WR in clock cycles as programmed in MR0.
Note 11. The maximum read postamble is bound by tDQSCK(min) plus tQSH(min) on the left side and tHZ(DQS)max on the right side. See “Clock to Data Strobe Relationship”.
Note 12. Output timing deratings are relative to the SDRAM input clock. When the device is operated with input clock jitter, this parameter needs to be derated by t.b.d.
Note 13. Value is only valid for RON34.
Note 14. Single ended signal parameter.
Note 15. tREFI depends on TOPER.
Note 16. tIS(base) and tIH(base) values are for 1V/ns CMD/ADD single-ended slew rate and 2V/ns CK, CK# differential slew rate. Note for DQ and DM signals, VREF(DC) = VRefDQ(DC). For input only pins except RESET#, VRef(DC) = VRefCA(DC). See “Address / Command Setup, Hold and Derating”.
Note 17. tDS (base) and tDH (base) values are for a single-ended 1 V/ns slew rate DQs and 2 V/ns slew rate differential DQS, DQS#; when DQ single-ended slew rate is 2V/ns, the DQS differential slew rate is 4V/ns. Note for DQ and DM signals, VREF(DC) = VRefDQ(DC). For input only pins except RESET#, VRef(DC) = VRefCA(DC). See “Data Setup, Hold and Slew Rate Derating”
Note 18. Start of internal write transaction is defined as follows:
- For BL8 (fixed by MRS and on- the-fly): Rising clock edge 4 clock cycles after WL.
- For BC4 (on- the- fly): Rising clock edge 4 clock cycles after WL.
- For BC4 (fixed by MRS): Rising clock edge 2 clock cycles after WL.

Note 19. The maximum read preamble is bound by tLZ(DQS)min on the left side and tDQSCK(max) on the right side. See “Clock to Data Strobe Relationship”.
Note 20. CKE is allowed to be registered low while operations such as row activation, precharge, autoprecharge or refresh are in progress, but power-down IDD spec will not be applied until finishing those operations.
Note 21. Although CKE is allowed to be registered LOW after a REFRESH command once tREFPDEN(min) is satisfied, there are cases where additional time such as tXPDLL(min) is also required. See “Power-Down clarifications-Case 2”.
Note 22. Defined between end of MPR read burst and MRS which reloads MPR or disables MPR function.
Note 23. One ZQCS command can effectively correct a minimum of 0.5 % (ZQ Correction) of RON and RTT impedance error within 64 nCK for all speed bins assuming the maximum sensitivities specified in the ‘Output Driver Voltage and Temperature Sensitivity’ and ‘ODT Voltage and Temperature Sensitivity’ tables. The appropriate interval between ZQCS commands can be determined from these tables and other application-specific parameters.
One method for calculating the interval between ZQCS commands, given the temperature (Tdriftrate) and voltage (Vdriftrate) drift rates that the SDRAM is subject to in the application, is illustrated. The interval could be defined by the following formula:

$$\frac{ZQCorrection}{(TSens \times Tdriftrate) + (VSens \times Vdriftrate)}$$

Where TSens = max(dRTTdT, dRONdTM) and VSens = max(dRTTdV, dRONdVM) define the SDRAM temperature and voltage sensitivities.
For example, if TSens = 1.5% / °C, VSens = 0.15% / mV, Tdriftrate = 1 °C / sec and Vdriftrate = 15 mV / sec, then the interval between ZQCS commands is calculated as:

$$\frac{0.5}{(1.5 \times 1) + (0.15 \times 15)} = 0.133 \approx 128ms$$

Note 24. n = from 13 cycles to 50 cycles. This row defines 38 parameters.
Note 25. tCH(abs) is the absolute instantaneous clock high pulse width, as measured from one rising edge to the following falling edge.
Note 26. tCL(abs) is the absolute instantaneous clock low pulse width, as measured from one falling edge to the following rising edge.
Note 27. The tIS(base) AC125 specifications are adjusted from the tIS(base) AC135 specification by adding an additional 75ps of derating to accommodate for the lower alternate threshold of 125 mV and another 10 ps to account for the earlier reference point [(135 mv - 125 mV) / 1 V/ns].
Note 28. Pulse width of a input signal is defined as the width between the first crossing of Vref(dc) and the consecutive crossing of Vref(dc).
Note 29. tDQSL describes the instantaneous differential input low pulse width on DQS - DQS#, as measured from one falling edge to the next consecutive rising edge.
Note 30. tDQSH describes the instantaneous differential input high pulse width on DQS - DQS#, as measured from one rising edge to the next consecutive falling edge.
Note 31. tDQSH, act + tDQSL, act = 1 tCK, act ; with tXYZ, act being the actual measured value of the respective timing parameter in the application.
Note 32. tDQSH, act + tDSS, act = 1 tCK, act ; with tXYZ, act being the actual measured value of the respective timing

parameter in the application.

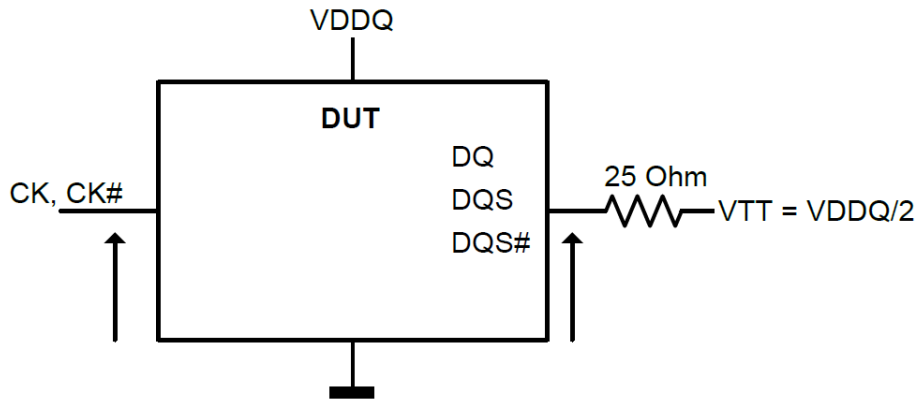
Note 33. The CL and CWL settings result in tCK requirements. When making a selection of tCK, both CL and CWL requirement settings need to be fulfilled

7 Reference Load for AC Timing and Output Slew Rate

The following figure represents the effective reference load of 25 ohms used in defining the relevant AC timing parameters of the device as well as output slew rate measurements.

It is not intended as a precise representation of any particular system environment or a depiction of the actual load presented by a production tester. System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment. Manufacturers correlate to their production test conditions, generally one or more coaxial transmission lines terminated at the tester electronics.

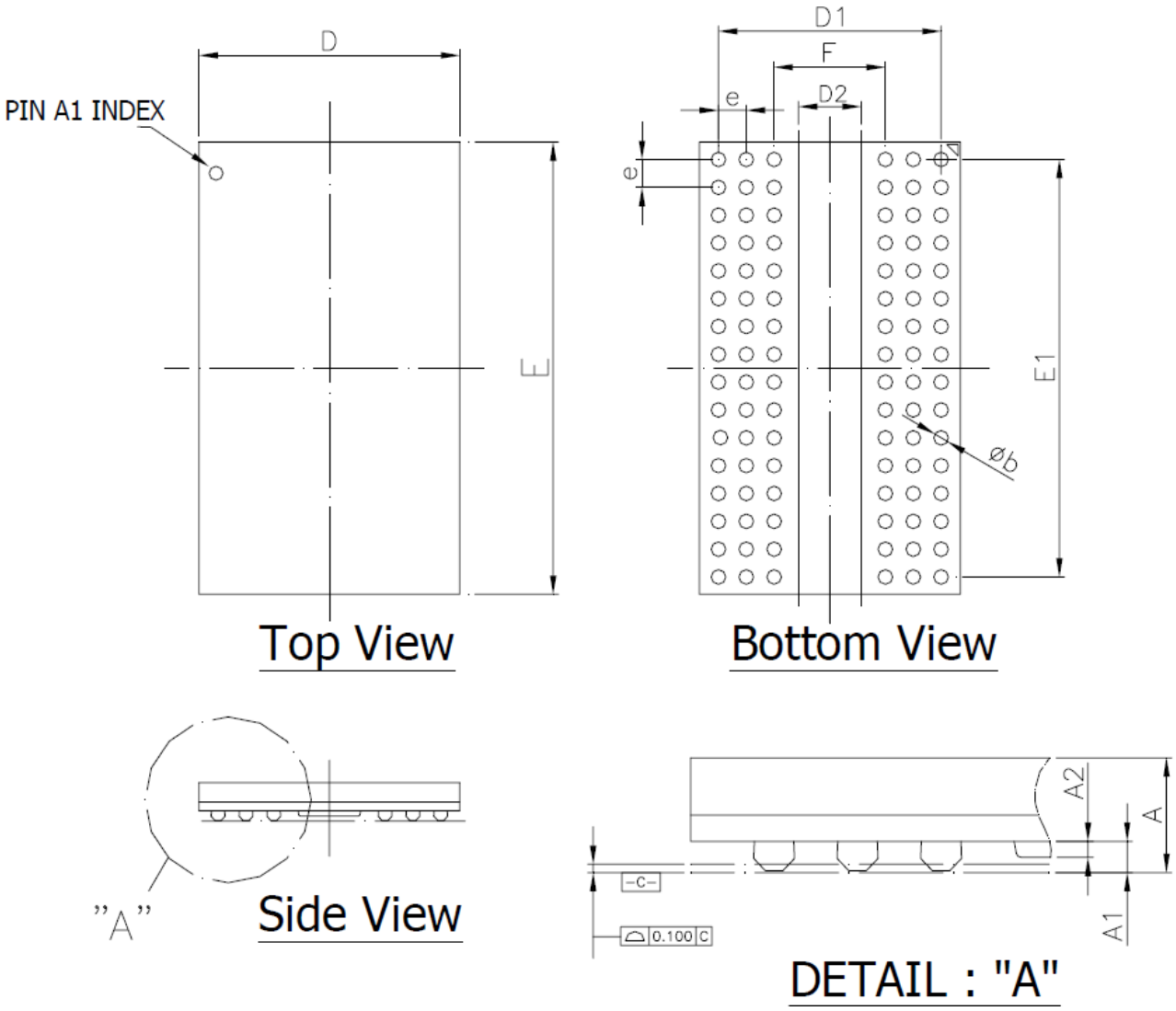
Figure 2 - Reference Load for AC Timings and Output Slew Rates



8 Package Outlines

Figure 3 reflects the current status of the outline dimensions of the DDR3 packages for 1Gbit component x16 configuration.

Figure 3 - 96-Ball FBGA Package 7.5x13x1.0 mm (max) Outline Drawing Information



Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	--	--	0.039	--	--	1.00
A1	0.010	--	0.016	0.25	--	0.40
A2	--	--	0.008	--	--	0.20
D	0.291	0.295	0.299	7.40	7.50	7.60
E	0.508	0.512	0.516	12.90	13.00	13.10
D1	--	0.252	--	--	6.40	--
E1	--	0.472	--	--	12.00	--
F	--	0.126	--	--	3.20	--
e	--	0.031	--	--	0.80	--
b	0.016	0.018	0.020	0.40	0.45	0.50
D2	--	--	0.081	--	--	2.05

9 Product Type Nomenclature

For reference the UniIC SDRAM component nomenclature is enclosed in this chapter

Table 5 - DDR3 Memory Components

Field	Description	Values	Coding
1	UniIC Component Prefix	SCB	UniIC
2	Voltage	13	VDD, VDDQ=1.35V (1.283V ~ 1.45V)
3	DRAM Technology	H	DDR3
4	Density	1G	1 Gbit
5	Number of I/Os	16	X16
6	Product Variant	0 .. 9	–
7	Die Revision	A	First
		B	Second
		C	Third
		D	Fourth
8	Package,	F	FBGA
9	Power	–	Standard power product
		L	Low power product
10	Speed Grade	15H	CL–Trcd–Trp = 9-9-9
		13K	CL–Trcd–Trp =11-11-11
		11M	CL–Trcd–Trp =13-13-13
11	Temperature Range	Blank	Commercial Temperature Range:0~95℃
		I	Industiral Temperature:-40~95℃

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